5/2/1

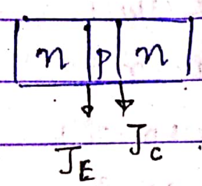
Module 2: Transistors..

Transistor is a 3-terminal device.

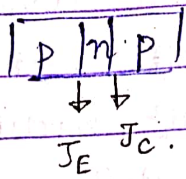
Transistor

- BJT — Bipolar junction Transistor
  - n-p-n
  - p-n-p..
- FET — Field Effect Transistor

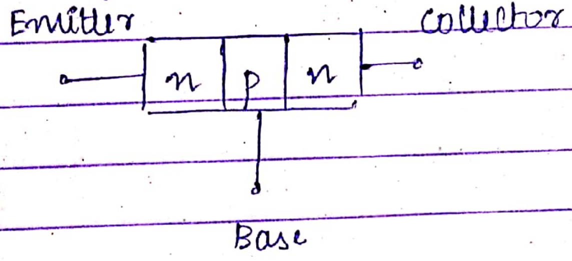
n-p-n



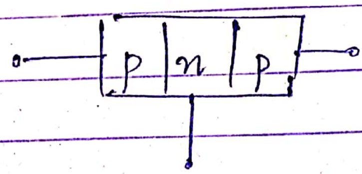
p-n-p..

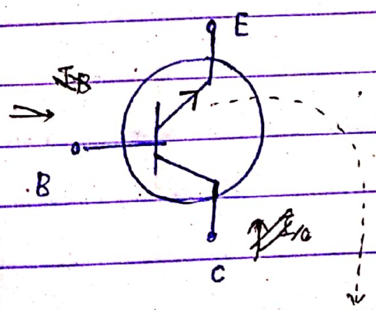


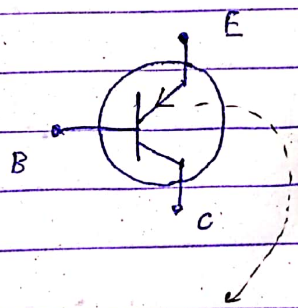
Symbol:



Symbol







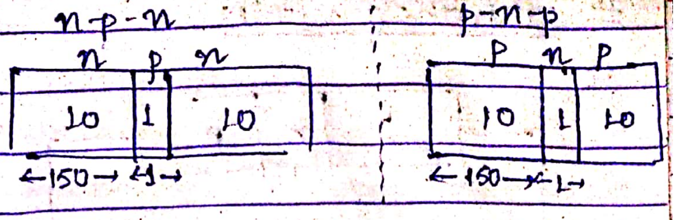
convention:
current flows outwards.

convention:
flows from the emitter inwards

just an assumptions.

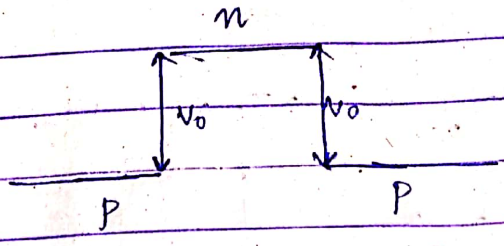
Doping ratio: $\boxed{1:10}$

size ratio: $\boxed{150:1}$



Generally length of emitter & collector is ~~ratio~~ taken same.

#



Borrier potential is same for both the junctions, until biasing is applied.

Modes of operation of a transistor:

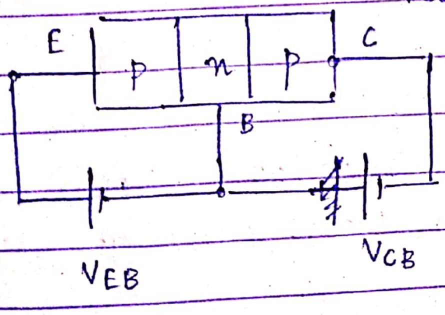
→ active mode

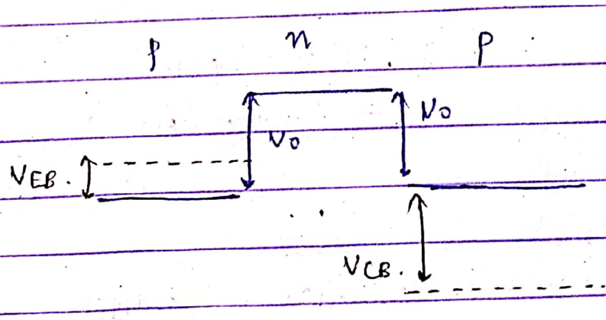
→ cut-off mode

→ saturation mode.

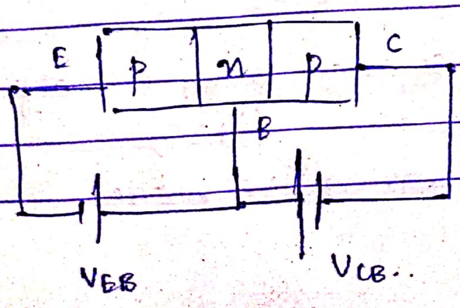
In active mode:

* Emitter-base junction is forward Biased & collector base junction is reversed bias.



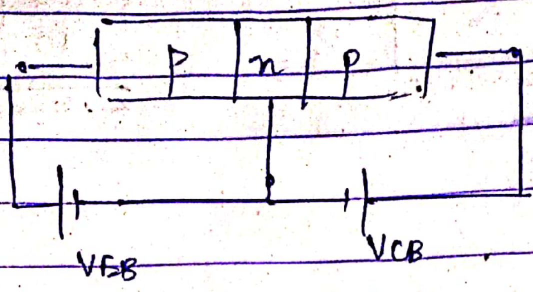


~~cutt~~ cut-off mode:



* Both the junctions are reversed bias

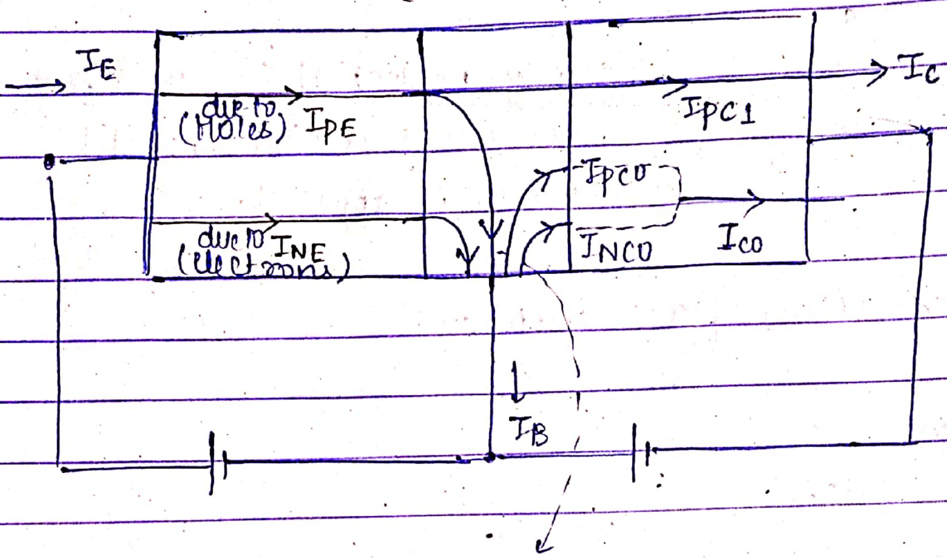
Saturation mode:



Both are forward biased.

Current components in p-n-p transistor:

(Active mode)



I_{NCO} (NC-open)

current due to recombination of holes & electrons.

$$\boxed{I_E = I_{PE} + I_{NE}}$$

$\therefore$ $I_C = I_{CO} + I_{PC1}$

$= I_{CO} + \alpha I_E$ ($\because$ some fraction of I_{PE} is reduced when holes & electrons recombine)

α: ratio of collector-current increment from cut-off region (i.e. reversed bias region) to the emitter-current change from cut-off region.

$I_C = I_{CO}$

($I_E = 0$)

$$\boxed{\alpha = \frac{I_C - I_{CO}}{I_E - 0}}$$

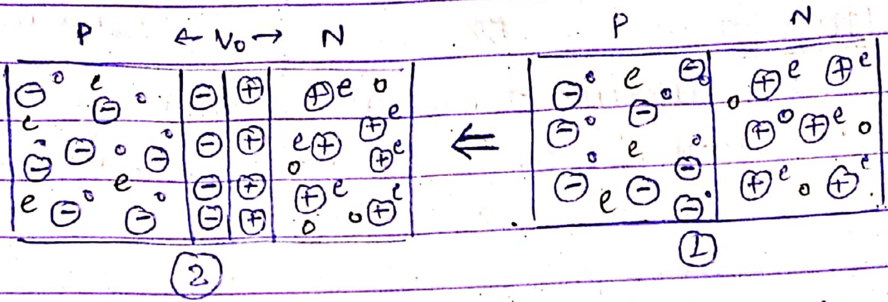
valid for active mode.

Generalised expression:

$$I_C = I_{CO}\left(e^{V/\eta V_T} - 1\right) + \alpha I_E.$$

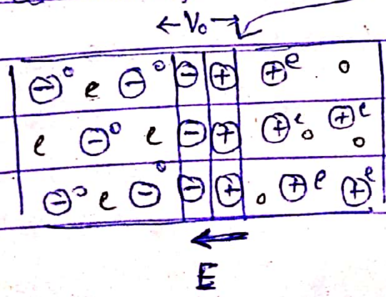
include energy band diagram.

Q Explain the concept of barrier potential. ~~# don't write~~ point-wise.



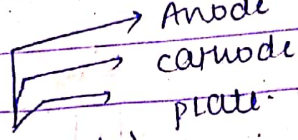
* When the same material is subjected to doping with acceptor type impurities in one half & donor type impurities in another half, ~~a PN junction gets created.~~ a PN junction gets created.
* The portion injected with acceptor type impurities has abundance of holes & hence in P type, holes are majority carriers.
* The other portion injected with donor type impurities has abundance of electrons & hence the N-side ~~is~~ has ~~a~~ electrons ~~with~~ as majority carriers.
* Both the P-side & N-side have minority carriers as electrons & holes respectively, generated via the breakage of covalent bonds due to thermal energy.
* Gradually, the holes ~~from the P-side move to the~~ from the P-side closer to the junction & electrons from N-side closer to the junction recombine to form a layer of immobile ions. These immobile ions restrict the further movement of electrons & holes.

*



* Thus, an electric field gets created from N to the P side.
* This gives rise to a potential gradient between the two sides, with a potential difference known as barrier potential. (V_0).

Transistor:



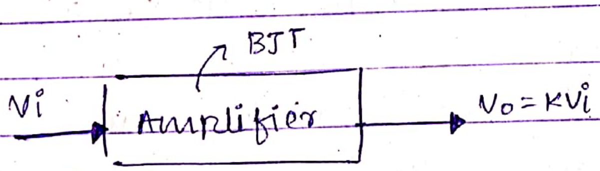
(Replacement of vacuum triode)

Both holes & electrons take part in conduction process, thus it is called "bipolar" transistor.

Transistor = Transfer + Resistor

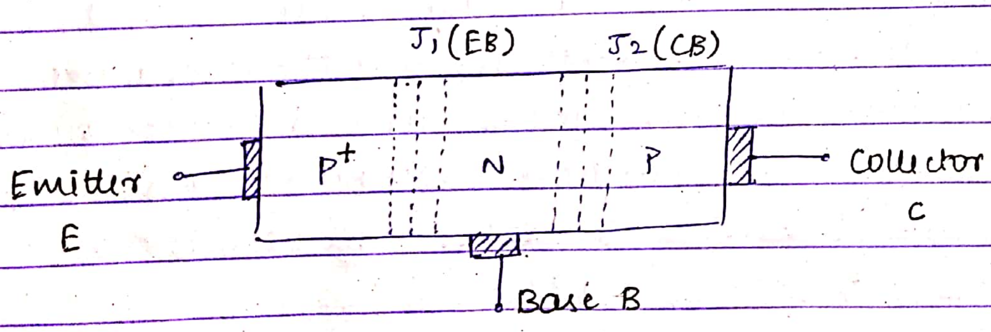
Addition of a third terminal, opened up possibilities for "weak signal strengthening." (or amplification)
BJT acts as a switch & ~~and~~ as amplifier.

#



$\therefore V_0 = KV_i$

$\boxed{\dfrac{V_0}{V_i} = K}$; K: amplifi~~cat~~cation factor.

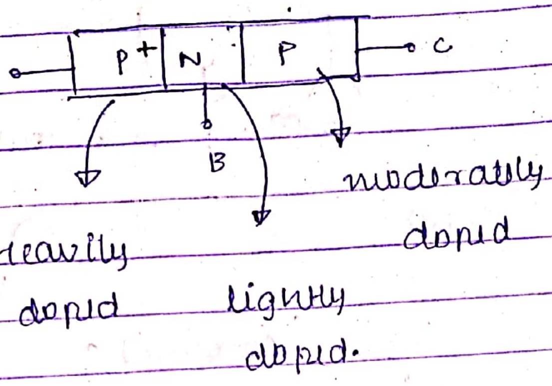


Three-terminal, three-layer, two junction semiconductor device: Transistor.

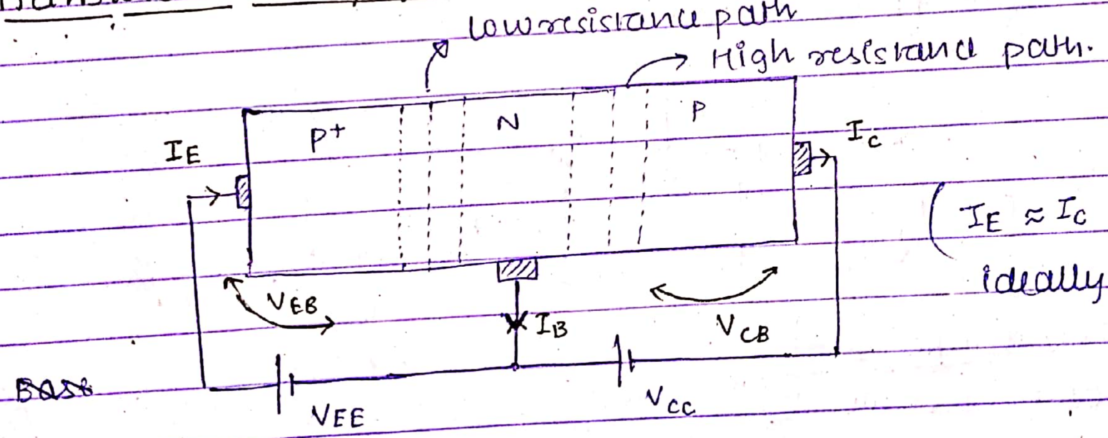
Boyle ~~stad~~ sted (BOOK)

J_{1EB}	J_{2CB}	Action
FB	FB	On state of a switch (saturation)
FB	RB	Amplification (Active region)
RB	FB	: inverted (though not a transistor action)
RB	RB	Off state of a switch (cut-off)

(size of) collector > (size of) emitter > (size of) base



Transistor as amplifier:



($I_E \approx I_C$) ideally

→ Base is narrow & lightly doped so that holes coming from emitter do not recombine at the base.

→ Holes immediately (though some recombine) pass to the collector region.

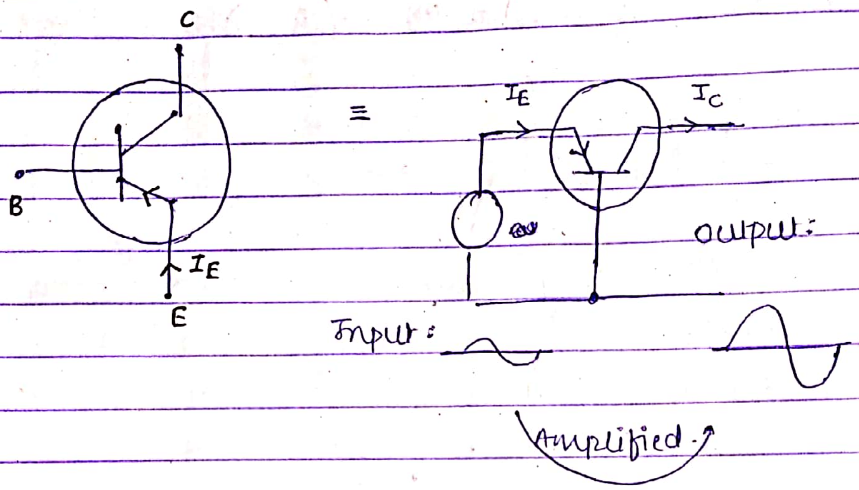
→ Direction of base current I_B: to compensate the electrons lost in recombination.

width of collector region is the Largest to dissipate large amount of heat

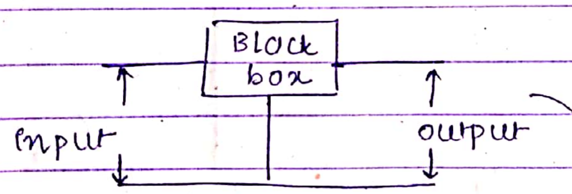
$\overset{\text{input current}}{I_E} = I_C + I_B$.

Transferring current from ~~rest~~ low resistance path to high resistance path: Transfer + resistor.

Symbol:



Any three terminal electronic device can be modelled as a "two-port network".

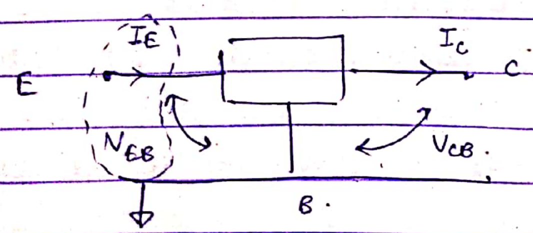


Possible configurations:

CB: common base

CE: common emitter

CC: common collector.



variables to study input characteristics.

zener break down depends upon electric field
strength.

constant

for different (V_{CB}) variation of V_{EB} with I_E : input characteristic.

Q:1. semiconductor has negative temperature coefficient of resistance.

2. If junction temperature increases to 10°c, the reverse saturation current doubles.

3. At absolute 0, intrinsic semiconductor behaves as an insulator.

4. If temperature increases, the extrinsic semiconductor behaves as intrinsic semiconductor with high conductivity.

5. zener breakdown voltage decreases with temperature increase.

If in a silicon diode, junction temperature increases, reverse saturation increases by 8% /°c] Theoretically calculated.

for germanium, it increases by 11% /°c

Practically, the increase in reverse saturation current for both germanium & silicon is 7% /°c.

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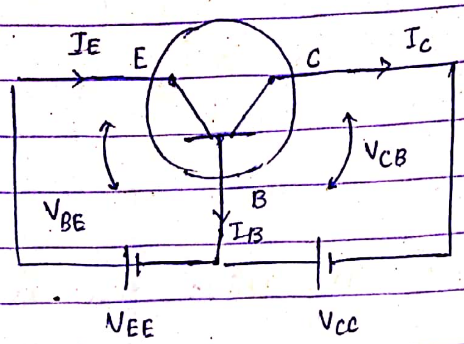
12/02/19.

Recombination occurs only in the base region in a transistor

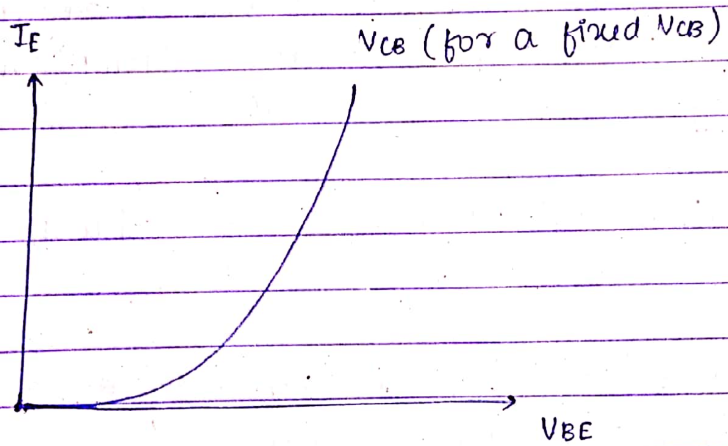
<u>Common Base:</u> (PNP Transistor)



Emitter-Base junction: forward biased & is the input port

★ $I_E = f(V_{BE}, V_{CB})$

∵ I_E ~~will~~ ~~can vary~~ can get affected because of voltage drop across CB terminal.



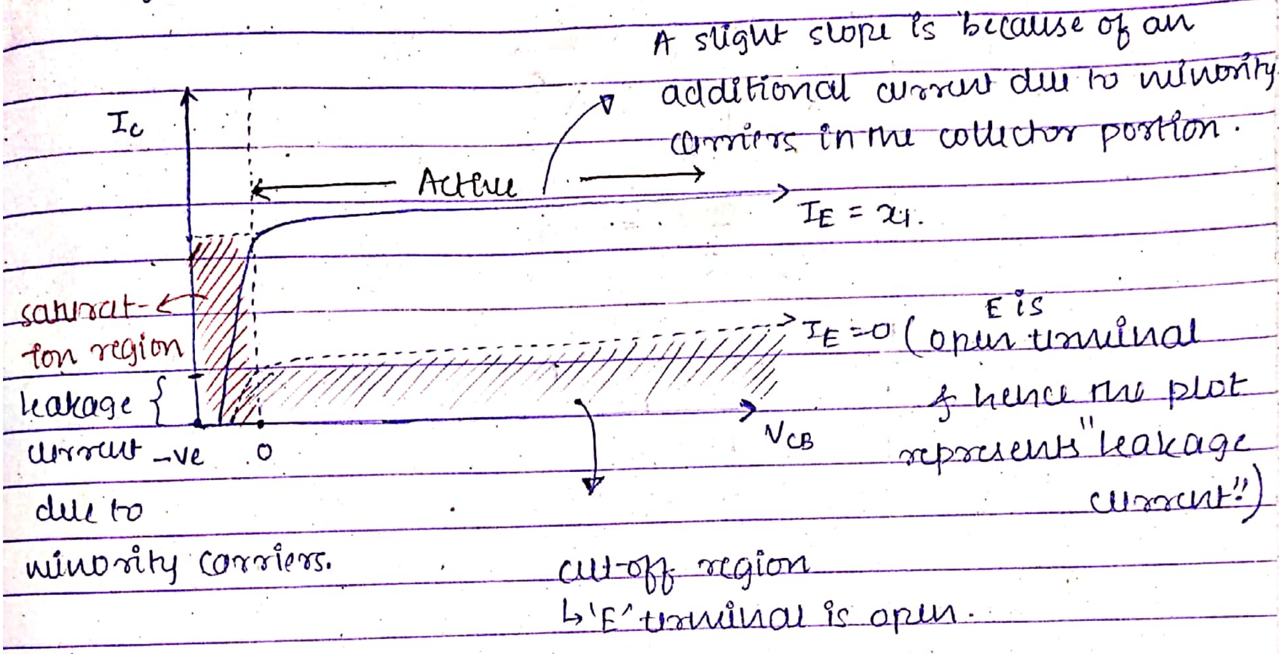
<u>Input-characteristics.</u>

On increasing V_{CB}, concentration of minority carriers increases. Thus, 'I_C' or collector current is a function of (emitter current + minority current). Thus, collector current increases & hence emitter current also increases.

$I_C = f$ (I_E, current due to minority carriers).

Output-characteristics:

* $I_C = f(V_{CB}, I_E)$: gives output characteristic of a transistor.
(I_E → fixed.)



In active region, collector current is almost independent of V_{CB}.

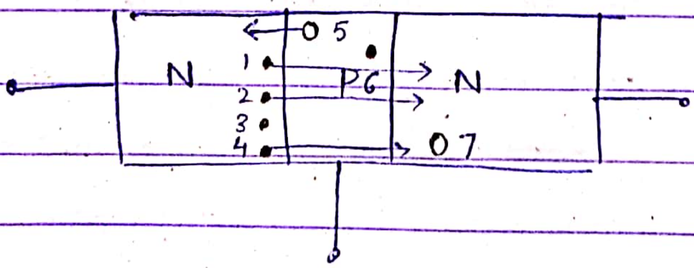
current will pass through emitter-base junction only if voltage crosses 0.7V.
while ~~at~~ the collector-base junction if has -0.7V, attains a forward-bias state. Thus, saturation occurs (∵ both junctions are forward biased)

fixed

$I_B = f(V_{BE}, V_{CE})$: input charachteristics

$I_C = f(V_{CE}, I_B)$: output characteristics

fixed



$$\boxed{\alpha_{dc} = \gamma \cdot \beta'}$$

α_{dc} : dc current gain in CB configuration.

γ : Emitter efficiency

β' : Base transportation factor

say,

say, Electrons 1, 2 & 4 reach the collector
Electron 3 recombines at base
Electron '6' & hole '7' constitute leakage current.

β': ratio of no. of electrons collected by the collector to the no. of electrons emitted by the emitter. (0.95 or greater)

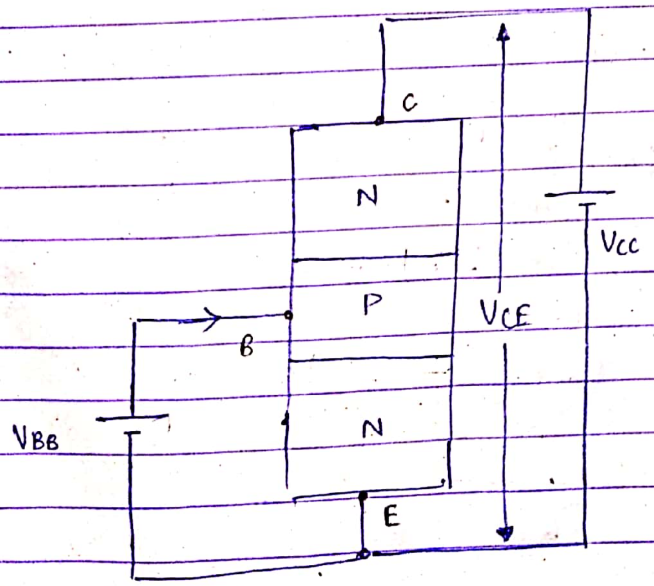
γ: ratio of emitter current to total current (0.95 or greater)

α_{dc} is generally ≈ 0.99.

$\therefore \boxed{I_C = \alpha_{dc} \cdot I_E + \underbrace{I_{CBO}}_{\text{leakage current}}}$

where, $I_E = I_C + I_B$.

Common Emitter:



voltage drop across J_{CB} = $V_{CE} - V_{BE}$

output characteristic
$I_C = f(I_B, V_{CE})$ fixed.
Input characteristic
$I_B = f(V_{BE}, V_{CE})$
constant

$I_C = \alpha_{dc} \cdot I_E + I_{CBO}$
$I_C = \alpha_{dc} (I_C + I_B) + I_{CBO}$

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$$I_C = \alpha_{dc} \cdot I_C + \alpha_{dc} \cdot I_B + I_{CBO}$$

$$I_C(1-\alpha_{dc}) = \alpha_{dc} \cdot I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha_{dc}}{1-\alpha_{dc}}\right) \cdot I_B + \frac{I_{CBO}}{1-\alpha_{dc}}$$

$$I_C = \underbrace{\left(\frac{\alpha_{dc}}{1-\alpha_{dc}}\right)}_{\beta_{dc}} \cdot I_B + \underbrace{\left(\left(\frac{1}{1-\alpha_{dc}}\right) \cdot I_{CBO}\right)}_{I_{CEO}}$$

$\therefore$ $\boxed{I_C = \beta_{dc} \cdot I_B + I_{CEO}}$ $\Rightarrow$ for common emitter

where, $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$ & $I_{CEO} = \frac{I_{CBO}}{1-\alpha_{dc}}$.

$\because$ I_{CEO} (leakage current) is very small,

$$\boxed{\therefore I_C = \beta_{dc} \cdot I_B}$$

$$\boxed{\therefore \beta_{dc} = \frac{I_C}{I_B}}$$

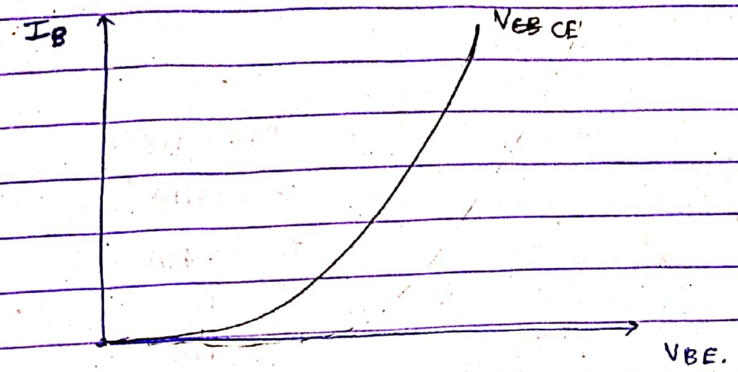
$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$\frac{1}{\beta_{dc}} = \frac{1-\alpha_{dc}}{\alpha_{dc}}$$

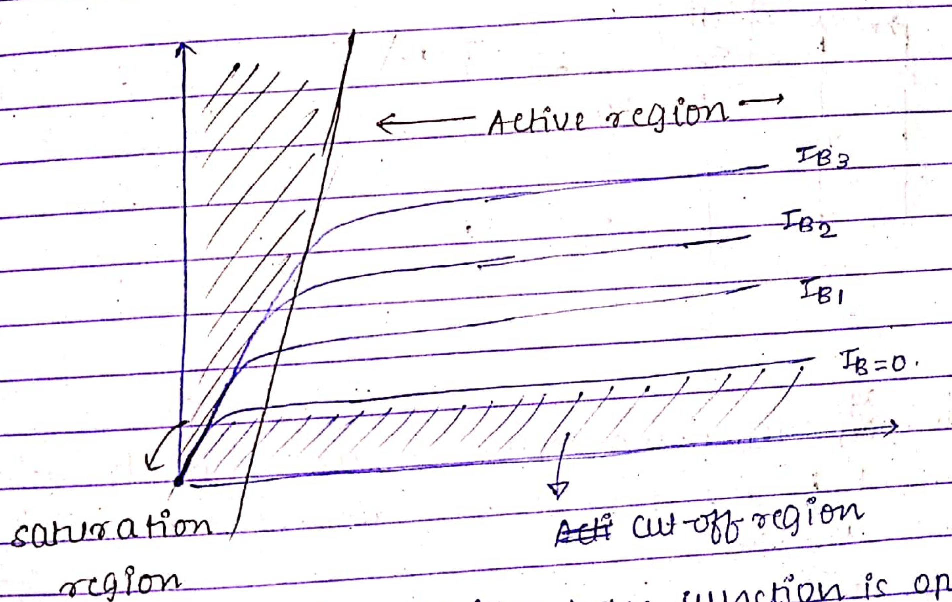
$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1 \Rightarrow \left(\frac{1}{\beta_{dc}} + 1\right) = \frac{1}{\alpha_{dc}}$$

$$\Rightarrow \boxed{\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc}+1}}$$

Input characteristic: (I_B vs V_{BE})

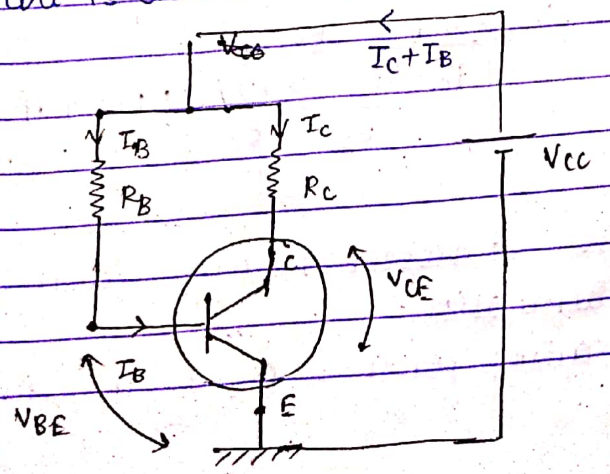


$I_{B3} > I_{B2} > I_{B1} > I_B.$



*. In cut-off region, emitter-base junction is open. Thus, the only current is due to leakage current = I_{CEO}.

Q



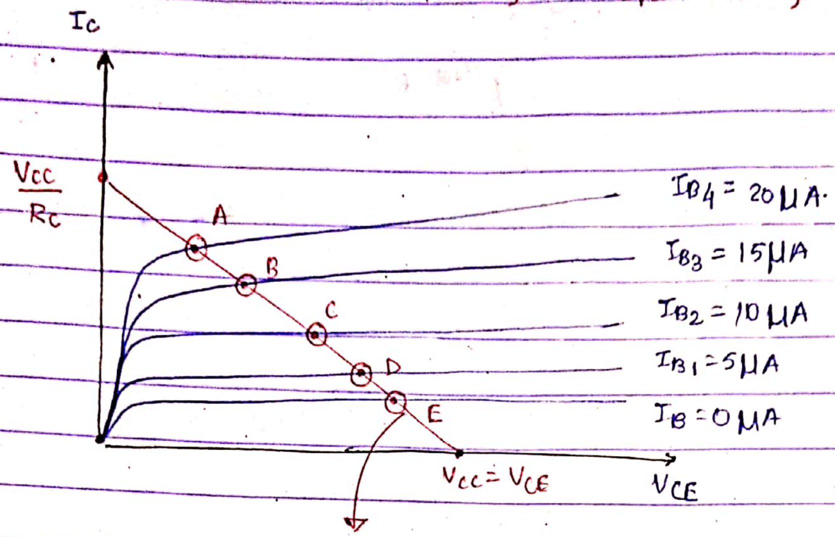
$V_{CC} = I_B R_B + \cancel{I_C R_C}\ V_{BE}$

$V_{CC} = I_C R_C + V_{CE}$

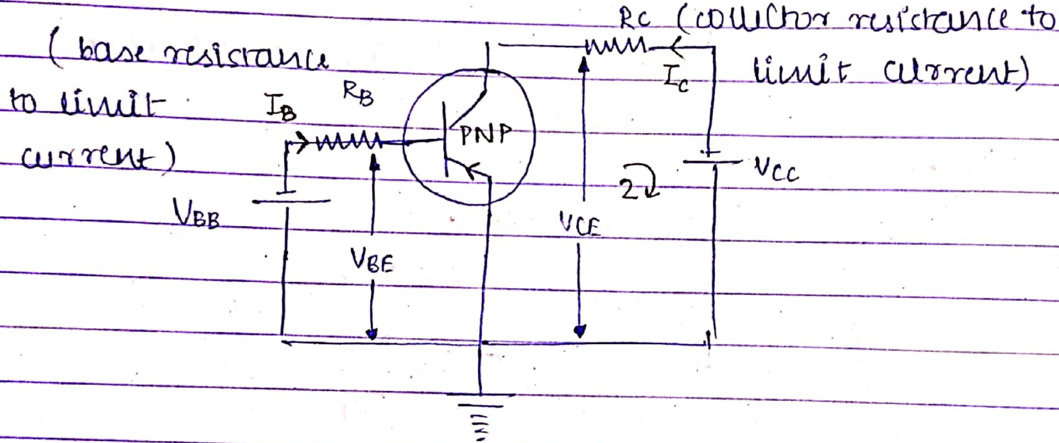
15/02/2019

Gain is very high in common-emitter config so it is most important.

A, B, C, D & E ≡ Operating points.



DC Load line



Thermal ~~Runway~~ Runaway : Damage of collector-base junction. (∵ I_{CBO} leakage current increases with increase in temperature)

~~$I_C R_C + V_{CC} = V_{CE}$~~

KVL in loop 2,

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CC} - V_{CE} = I_C R_C$$

$$\boxed{I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}}$$ ⇒ Load line.

usually Q-point is chosen in the middle of the ~~load~~ active region ~~line~~ to avoid attenuation.

once the operating point is fixed, it is called Q-point.

300Hz – 3.4 kHz – voice signals.
(or 4 kHz)

Any fluctuations in voltage, load resistance or temperature should'nt affect Q-point. It remains stable (ideally). Irrespective of any internal parameters, the Q-point remains fixed.

$\frac{V_o}{V_i}$ = amplification factor (voltage gain when the ratio is between voltages)
(current gain when ratio is between currents)

Transistor biasing helps in fixing Q-point.

V_{BE} decreases by 2.5 mV per °C.

20/02/2019

Q Write the 3 requirements of transistor biasing.

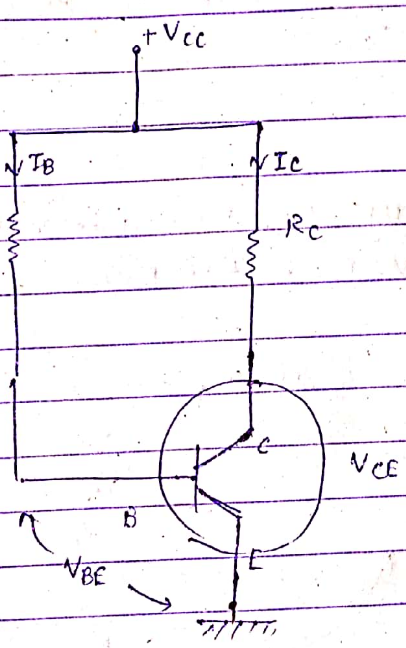
→ Emitter-base junction should be forward biased & collector base junction should be reversed bias.

→ operating point should be chosen in the middle of the active region. —(1).

→ Q-point or the operating point should be fixed i.e. it should be stable & independent of any other parameter.

→ on changing transistor, Q-point shouldn't shift.

Fixed biasing circuitory:



$V_{CC} = I_C R_C + V_{CE}$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

$I_B = \frac{V_{CC}}{R_B}$.

$I_C = \beta \cdot I_B + I_{CEO}$

& $I_{CEO} = (\beta+1) I_{CBO}$.

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$.

$I_C = f(\underbrace{I_{CO}, V_{BE}, \beta}_{})$

All are the functions of temperature

$$\therefore \frac{\partial I_C}{\partial} \quad \frac{dI_C}{dT} = \underbrace{\frac{\partial I_C}{\partial I_{CO}}}_{S} \cdot \frac{dI_{CO}}{dT} + \underbrace{\frac{\partial I_C}{\partial V_{BE}}}_{S'} \cdot \frac{dV_{BE}}{dT} + \underbrace{\frac{\partial I_C}{\partial \beta}}_{S''} \cdot \frac{d\beta}{dT}$$

$$\boxed{\therefore S = \frac{\partial I_C}{\partial I_{CO}} ; \quad S' = \frac{\partial I_C}{\partial V_{BE}} \quad \& \quad S'' = \frac{\partial I_C}{\partial \beta}.}$$

$I_C = \beta \cdot I_B + I_{CEO}$

$= \beta \cdot \left(\frac{V_{CC}-V_{BE}}{R_B}\right) + (\beta+1) I_{CBO}$

(demerit of this circuit)

$\therefore \frac{\partial I_C}{\partial I_{CBO}} = (\beta+1)$: compared to leakage current, I_C increases 50 times faster.

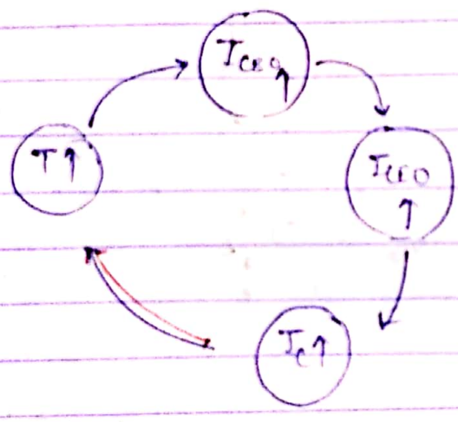
Thermal stability

stability can be achieved

$\frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B}$: stable when R_B is very large

$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}-V_{BE}}{R_B} + I_{CBO}$. R_B should be large.

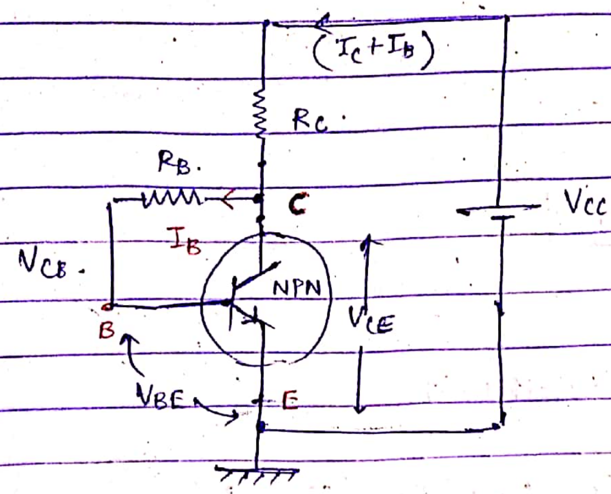
Thermal Runaway: On increasing temperature transistor gets damaged due to the following: ~~phenom~~



Heat = $I_C^2 \cdot R$

∵ Fixed biasing circuitry has no control over I_C, ∴ it is highly prone to thermal run-away. Thus, it is rarely used.

Collector-to-Base bias circuitory: (Voltage-feedback circuit)



$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$.

$V_C + (I_C + I_B) R_C - V_{CC} = V_E$

$V_C - V_E = V_{CC} - R_C (I_C + \cancel{I_B})$

$V_{CE} = V_{CC} - R_C (I_C + I_B) \Rightarrow V_{CE} = V_{CC} - I_C R_C - I_B R_C$ — (1)

or

$V_{CE} = I_B R_B + V_{BE}$ — (2) $\Rightarrow$ ~~$I_B R_B = V_{CE} - V_{BE}$~~

$\dfrac{V_{CE} - V_{BE}}{R_B} = I_B$

&

$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$ — (3)

~~$V_{CC} = (I_B + I_C) R_C$~~

$V_{CC} = (I_B + I_C) R_C + \cancel{I_B} \cdot \dfrac{(V_{CE} - \cancel{V_{BE}})}{\cancel{I_B}} + \cancel{V_{BE}}$

$V_{CC} = I_B R_C + I_C R_C + V_{CE}$

$I_B = \dfrac{V_{CC} - V_{CE} - I_C R_C}{R_C}$

$I_B = \dfrac{V_{CC}}{R_C} - \dfrac{V_{CE}}{R_C} - I_C$.

From (2), $V_{CC} - V_{BE} - I_C R_C = I_B (R_C + R_B)$

$\therefore I_B = \dfrac{V_{CC} - V_{BE} - I_C R_C}{(R_C + R_B)}$

Equation (1), is

$$V_{CC} - V_{CE} = (I_B + I_C) R_C$$

$\because I_B + I_C = I_E$,

$\therefore V_{CC} - V_{CE} = I_E \cdot R_C$.

$$\Rightarrow \boxed{I_E = \frac{V_{CC} - V_{CE}}{R_C}}$$

Also eqn (1) can be written as

$$V_{CC} - V_{CE} = (I_B + \beta \cdot I_B) R_C \quad (\because I_C = \beta \cdot I_B)$$

$$V_{CC} - V_{CE} = (1+\beta) I_B \cdot R_C$$

$$\boxed{I_B = \frac{V_{CC} - V_{CE}}{(1+\beta) \cdot R_C}} \text{ — (A)}$$

Equation (3) similarly can be written as

$$V_{CC} - V_{BE} = I_B R_B + (I_B + I_C) R_C$$

$$\Rightarrow V_{CC} - V_{BE} = I_B R_B + (I_B + \beta \cdot I_B) \cdot R_C$$

$$\Rightarrow V_{CC} - V_{BE} = I_B [R_B + R_C + \beta R_C]$$

$$\therefore \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_C (1+\beta) + R_B}} \text{ — (B)}$$

equations (A) & (B) are same.

$\because I_C = \beta I_B + I_{CEO}$

$$\therefore I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_C(1+\beta) + R_B} \right] + I_{CEO} \quad (\text{from (B)})$$

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$$I_C = \beta\left[\frac{V_{CC}-V_{BE}}{(1+\beta)R_C+R_B}\right]+(\beta+1)\cdot I_{CBO} \quad (\because I_{CEO}=(\beta+1)I_{CBO}).$$

$$\therefore \frac{\partial I_C}{\partial I_{CBO}} = (\beta+1).$$

$$I_B = \frac{V_{CC}-V_{BE}-I_{CEO}\cdot R_C}{(1+\beta)R_C+R_B}$$

$$I_C = \beta\left[\frac{V_{CC}-V_{BE}-(\beta+1)R_C\cdot I_{CBO}}{(1+\beta)R_C+R_B}\right]+(\beta+1)I_{CBO}$$

$$\therefore \frac{\partial I_C}{\partial I_{CBO}} = \frac{-\beta\cdot(\beta+1)R_C}{(1+\beta)R_C+R_B}+(\beta+1)$$

$$= (\beta+1)\left[\frac{-\beta R_C}{(1+\beta)R_C+R_B}+1\right]$$

$$= (\beta+1)\left[\frac{-\cancel{\beta R_C}+R_C+\cancel{\beta R_C}+R_B}{(1+\beta)R_C+R_B}\right]$$

$$= \frac{(\beta+1)(R_C+R_B)}{(\beta+1)R_C+R_B}.$$

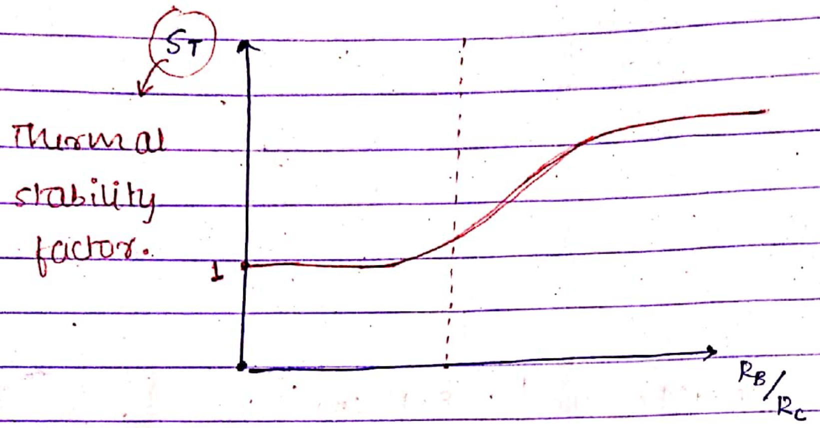
Dividing numerator & denominator by (R_C+R_B)

$$\frac{(\beta+1)}{(\beta+1)\frac{R_C}{R_C+R_B}+\frac{R_B}{R_C+R_B}} = \frac{(\beta+1)}{\frac{\beta\cdot R_C}{R_C+R_B}+1}.$$

$$\boxed{\frac{\partial I_C}{\partial I_{CBO}} = \frac{(\beta+1)}{1+\frac{\beta\cdot R_C}{R_C+R_B}}} = \frac{\beta+1}{1+\frac{\beta}{1+(R_B/R_C)}}$$

Higher the stability factor,

If R_B/R_C is very small, stability factor becomes 1. But if the ~~stt~~ ratio R_B/R_C increases, stability decreases.



Demerit: $\frac{\partial I_c}{\partial \beta} =$

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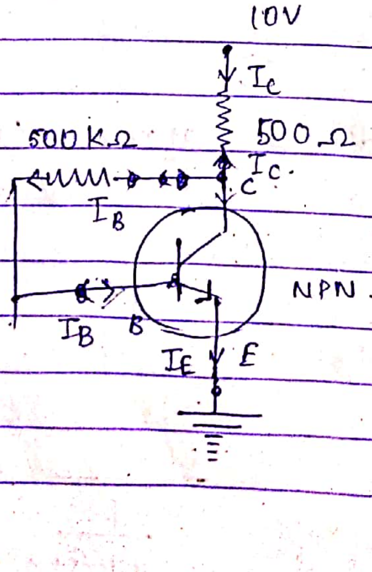
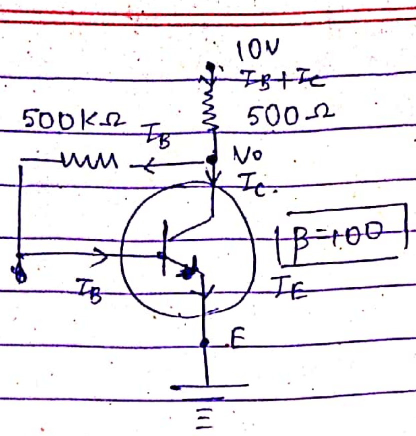
Q How much is the emitter current in the circuit? Also calculate ~~the~~ V_{CE}.



$10+500 \cdot I_C = V_C$

$V_C = 10+ 500 \cdot I_c$.

$10+500 \cdot I_c$



$I_E = I_B + I_C$.

$10 - 500(I_B + I_C) = V_o$.

$$I_B = \frac{V_{CC} - V_{BE}}{R_C(1+\beta) + R_B}.$$

~~V_o~~ $500K\, I_B$

$$\frac{V_{CC} - V_{BE}}{R_C + \beta R_C + R_B}.$$

After approximations:

$V_{CC} >> V_{BE}$ & $R_C << \beta R_C$

$\Rightarrow V_{CC} - V_{BE} \approx V_{CC}$ & $R_C + \beta R_C = \beta R_C$

$$\therefore I_B = \frac{V_{CC}}{R_B + \beta R_C}.$$

$$= \frac{10}{500\times10^3 + 100\times500}. \quad = \frac{10}{500(10^3 + 100)}$$

$$= \frac{10}{500\times10^2(10+1)}$$

$$= \frac{1}{5000(11)}$$

$$= \frac{1}{55\times10^3}$$

$$= \frac{1}{55}\times10^{-3}\,A.$$

$= 0.018\times10^{-3}\,A.$

$\therefore = 18\,\mu A.$

$I_B = 18\mu A$

$\therefore I_C = \beta \cdot I_B$

$= 100\times18\mu A$

$= 100\times18\times10^{-6}$

$= 18\times10^{-4}$

$= 1.8\,mA$.

$V_{CE} = V_{CC} - I_C R_C$.

$= 10 - 18\times10^{-4}\times500$

$= 10 - 9000\times10^{-4}$

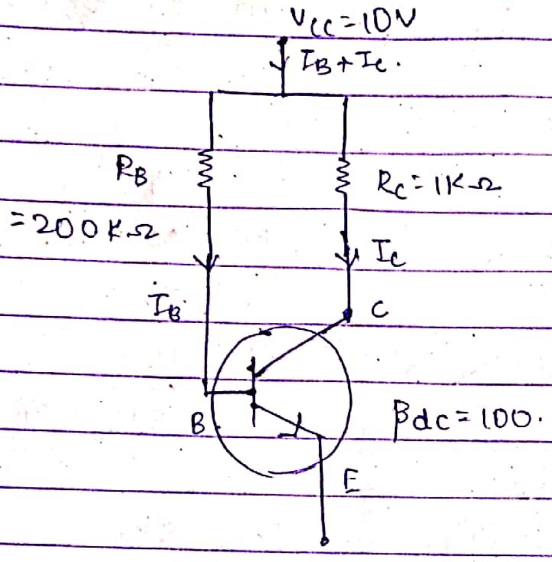
$= 10 - 0.9$

$\boxed{V_{CE} = 9.1V}$

$\because V_{CE} \approx V_{CC}$, $\therefore$ operating point is towards cut-off point.

If $V_{CE} = \cancel{5/10}$ 5V, then operating point lies in middle of active region.

Q. Calculate the value of V_{CE} in a fixed bias circuit. Given, $\beta_{dc} = 100$, $R_B = 200k\Omega$, $V_{CC} = 10V$



$$\boxed{I_C = \beta_{dc} \cdot I_B}$$

$\cancel{10 - I_B (200k) = V_B}$ $\cancel{10 - I_C (1k) = V_C}$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} = \frac{1\cancel{0}}{20\cancel{0}\,k}$$

$$\frac{1}{20} \times 10^{-3}$$

$$\frac{1}{2} \times 10^{-4} = \cancel{5\times} \; 0.5 \times 10^{-4}$$

$I_C = \beta_{dc} \cdot I_B$

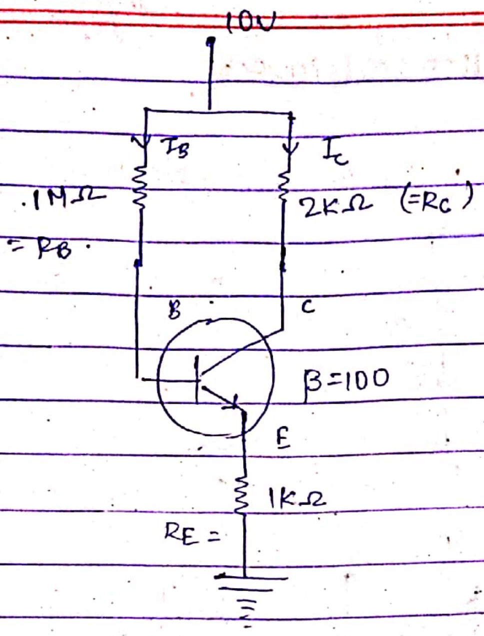
$= 5 \times 10^{-5} \times \cancel{5 \times 10^{-5}}\; 100$

$I_C = 5 \times 10^{-3}$

$V_{CE} = 10 - 5 \times \cancel{10^{-3}} \cdot \cancel{10^{3}}$

$= 5V.$

Q.



Q. For a certain transistor $\alpha_{dc} = 0.98$ & emitter current $I_E = 2mA$. calculate the value of base current I_B & I_C

Q. A transistor is supplied with DC voltage so that $I_B = 40\mu A$. If $\beta_{dc} = 80$, and leakage current is $5\mu A$. what is the value of emitter current I_E?

Ix -

Q. A transistor is connected in CB configuration. When the emitter voltage is changed by 200 mV the emitter current changes by 5mA. During this variation, the collector to base voltage is kept fixed. calculate the input dynamic resistance.

Generally, input resistance is very low in transistor.

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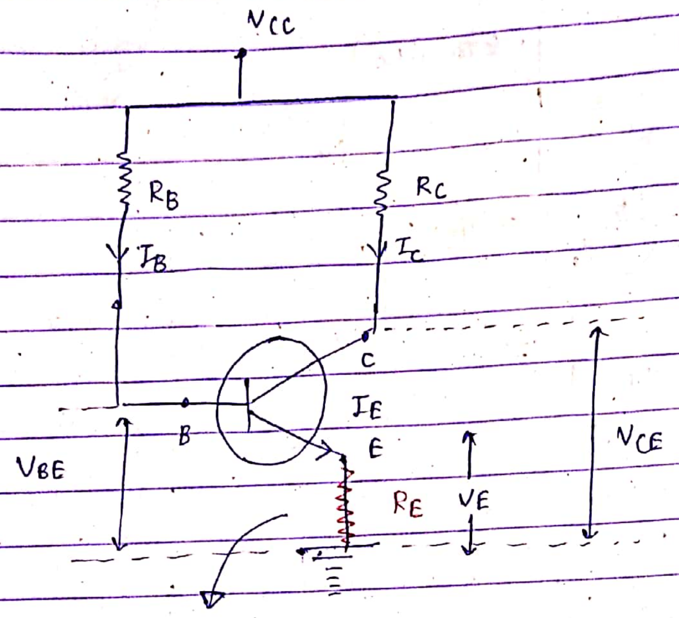
Fixed-Bias circuit with emitter resistance:



Input-loop circuit gives:

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E.$$

$$I_C = \beta I_B + I_{CEO}$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$

$$I_C = \frac{\beta}{(\beta+1)} I_E + I_{CBO}.$$

$$\frac{\beta}{(\beta+1)} I_E + \cancel{I_{CBO}} = \beta \cdot I_B + \beta \cdot I_{CBO} + \cancel{I_{CBO}}$$

$$\frac{\cancel{\beta} I_E}{\beta+1} = \cancel{\beta}(I_B + I_{CBO})$$

$$I_E = (\beta+1)(I_B + I_{CBO})$$

$$\Rightarrow I_E = I_B(\beta+1)$$

$$\therefore V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E.$$

$$V_{CC} - V_{BE} = I_B [R_B + (\beta+1) R_E]$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}$$

$$\boxed{I_B \approx \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}}$$ ⇒ After approximation

$$I_C = \beta \cdot I_B + I_{CEO}$$

$$\boxed{I_C = \beta \cdot \left(\frac{V_{CC} - V_{BE}}{R_E + \beta R_E}\right) + (\beta+1) I_{CBO}}$$

$$\Rightarrow \beta \Big(V_{cc+}$$

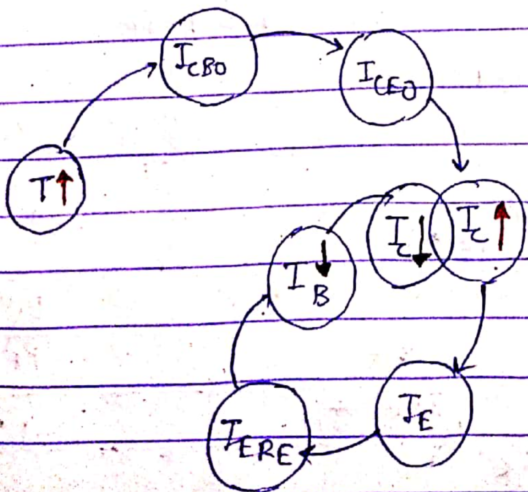
From output loop eq^n:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E.$$

$$\boxed{\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E.}$$

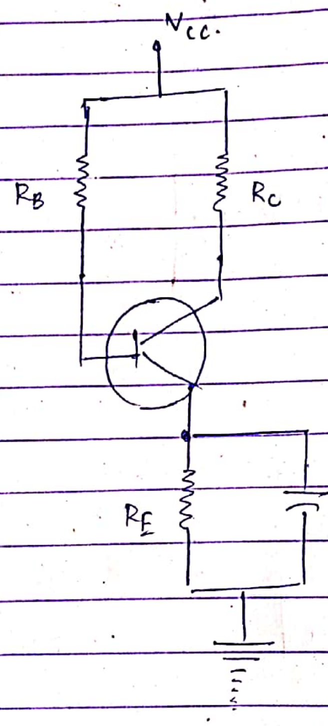
Effect of Temperature increase:



Demerit:

Emitter resistance is between input & output. Some output voltage is feeded back to input side & thus overall voltage gain defined by $\left(\frac{V_{output}}{V_{input}}\right)$ reduces.

To avoid this problem, a capacitor is placed in parallel with emitter resistance which provides a low ~~resistance~~ reactance path to AC variations or AC signals.



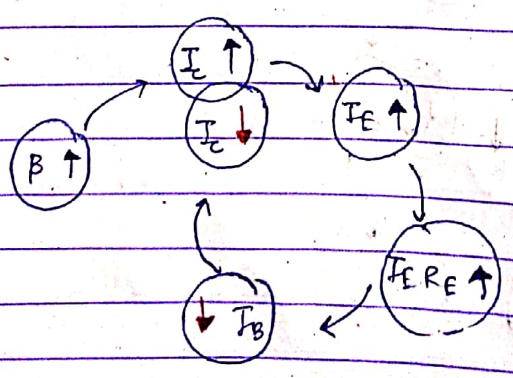
C_E (By-pass capacitor)
↳ Helps maintain the gain of the amplifier.

Effect of changing β:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_E} \qquad I_C = \beta \cdot I_B$$

$$\& \quad I_C = \frac{\beta(V_{CC} - V_{BE})}{R_B + (\beta+1)R_E}$$

$$= \frac{\frac{\beta}{R_B}(V_{CC} - V_{BE})}{1 + (\beta+1)\frac{R_E}{R_B}}$$

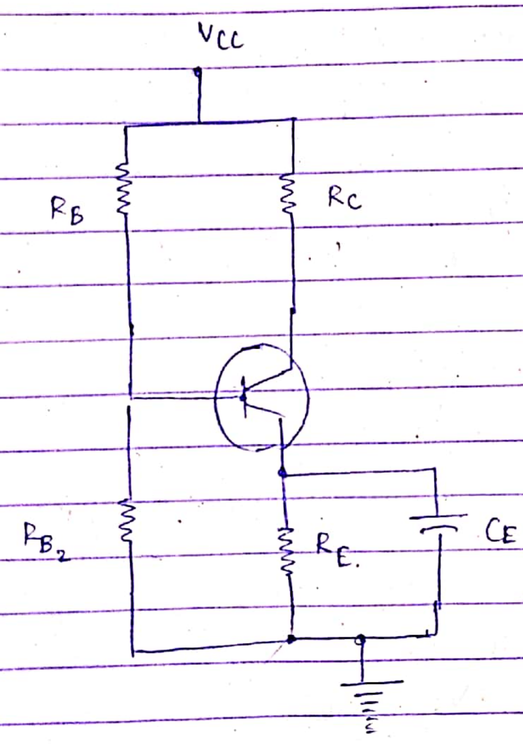


$R_E >>> \frac{R_B}{\beta}$

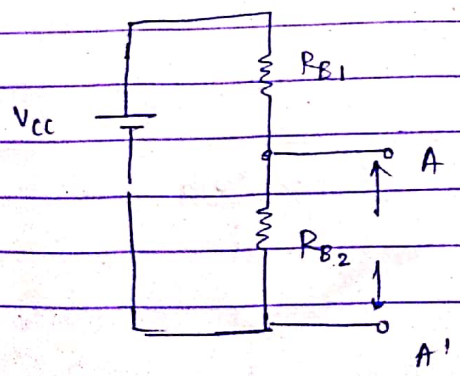
Why this circuitory (with capacitor) is also not used?

This circuitory is also not used because R_E should be much much greater than $\frac{R_B}{\beta}$. This cannot be achieved with one power supply. The base resistance 'R_B' must be given low power supply & 'R_C' must be given high power supply. Thus, it is not used.

Voltage-Divider circuit:



Using Thevenin's theorem,

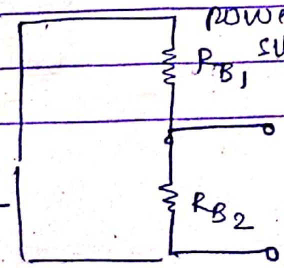


$$V_{Th} = \frac{R_{B_2} \cdot V_{CC}}{R_{B_1}+R_{B_2}}$$

And

(short circuiting power supply)

$$R_{Th} = \frac{R_{B_1} \cdot R_{B_2}}{R_{B_1}+R_{B_2}}$$



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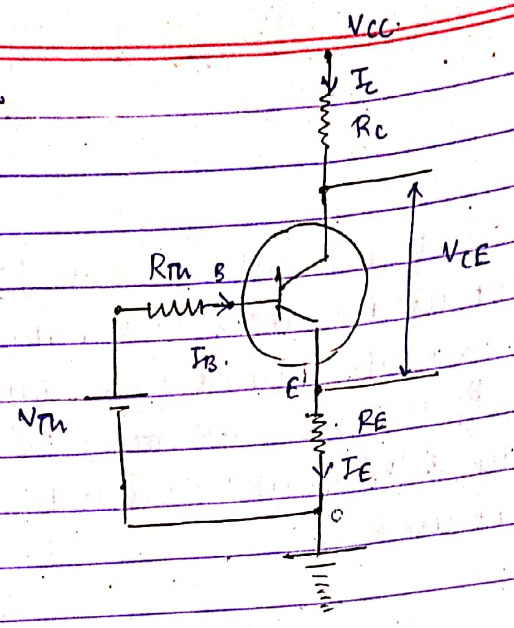


$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + \beta R_E}$$

$$V_{CC} - I_C R_C + I_B R_{Th} - V_{Th} = 0$$

$$\cancel{V_{CC} - I_C R_C - V}$$

$$I_B R_{Th} = I_C R_C + V_{Th} - V_{CC}$$

$$I_B =$$

$$V_B + I_B R_B - V_{Th} + I_E R_E = V_E$$

$$V_{BE} + I_B R_B - V_{Th} + I_E R_E = 0$$

$$R_{Th} I_B = V_{Th} - V_{BE} - I_E R_E$$

$$I_B = \frac{V_{Th} - V_{BE} - I_E R_E}{R_{Th} \cdot I_B}$$

$$= \frac{V_{Th} - V_{BE} - (\beta+1) I_B \cdot R_E}{R_{Th} \cdot I_B}$$

$$R_{Th} I_B + (\beta+1) I_B \cdot R_E = V_{Th} - V_{BE}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

$$\boxed{I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + \beta R_E}}$$

$$R_E >>> \frac{R_{Th}}{\beta}$$

Q-point can be fixed

Advantages & disadvantages of transistor biasing circuitories

* Demerit of fixed bias circuitory:
  Thermal runaway, as there is no control over I_C.

* Merit of fixed bias circuitory:
  - simple circuit with lesser components.
  - connection is easy

* Demerits of collector-to-base bias circuit:
  - some amount of output voltage is feeded back to input side. Thus ~~feed~~ voltage gain reduces.

* Merits of collector-to-base bias circuit:
  - controls thermal runaway to some extent
  - simple connection
  - lesser components

• Demerits of ~~voltage-divider~~ fixed bias circuitory with R_E.
  - Emitter resistance acts as a feedback resistance thus reducing voltage gain.

• Merits of fixed bias circuitory with R_E
  - can control thermal runaway.
  - control over β variations.

Demerits of fixed-bias circuitory with R_E & C_E.
- To ensure much greater R_E than $\frac{\beta}{R_B}$, two power supplies have to be used.

Merits of fixed-bias circuitory with R_E & C_E:
- Helps maintaining voltage gain.

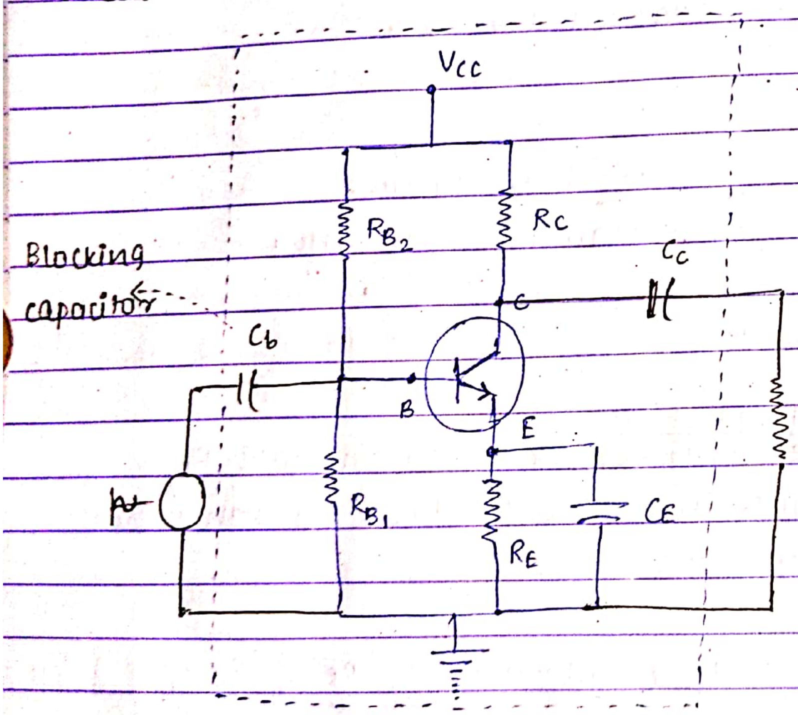
Demerits of voltage-divider circuitory:

- expensive
- complex connection with use of more no. of passive elements.

Merits of voltage-divider circuitory:

- stabilises Q point.

After certain modifications in the voltage-divider biasing, the circuit becomes an amplifier:



CE Amplifier circuit:

A blocking capacitor is used in the input side to block 'DC' output. Also so that any effect of Vcc on input AC signals is not seen. Similarly, a blocking capacitor is applied at the output as well.

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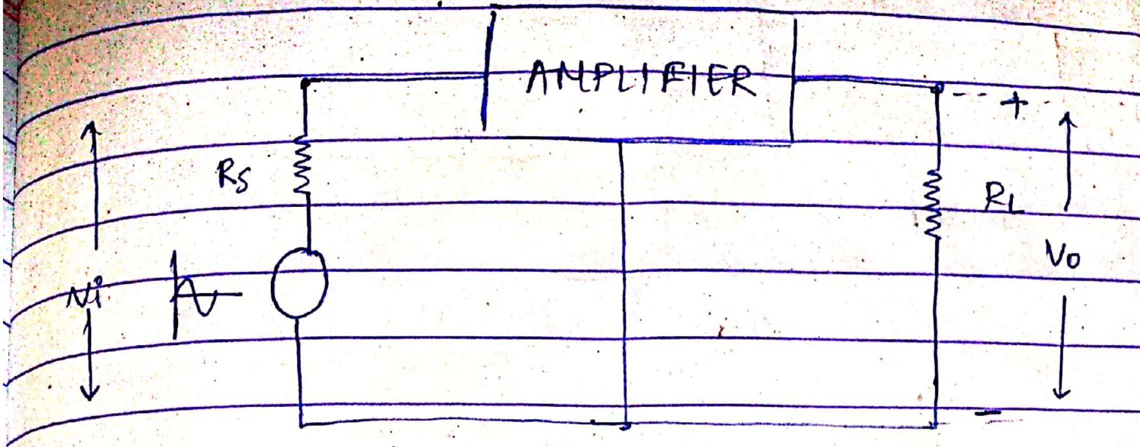
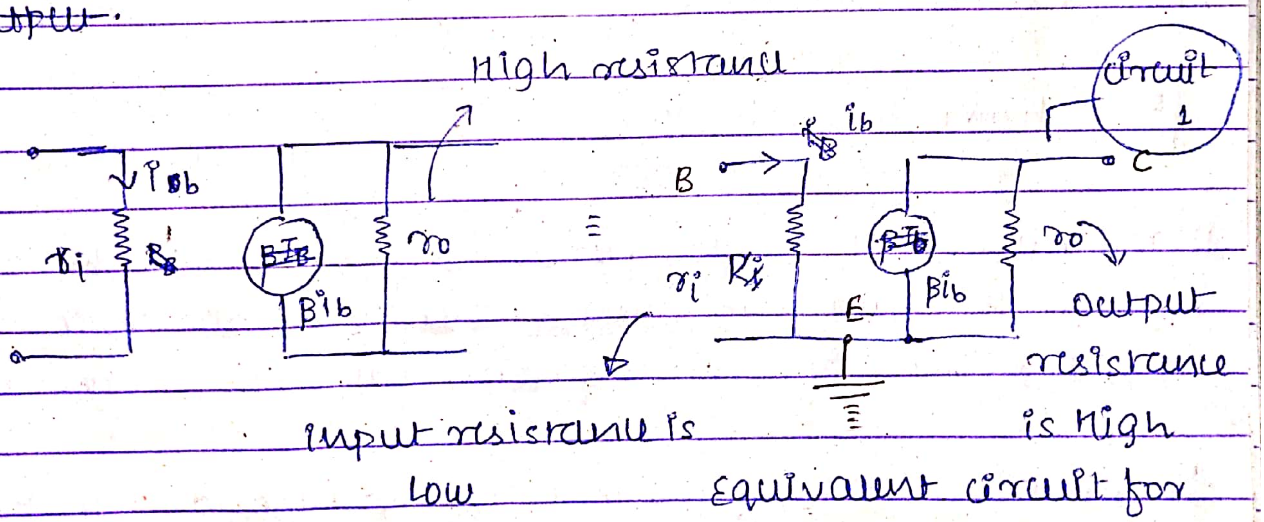


voltage gain $= A_v = \dfrac{V_o}{V_i}$

voltage gain with change in frequencies of input signals is the frequency response.

Graphical analysis is used for high power amplifiers. Thus, we can analyse using equivalent circuit of amplifier.

Transistor is just like a current-controlled source ~~at the output~~.



Equivalent circuit for transistor.

when small alphabets are used in subscript it denotes AC.

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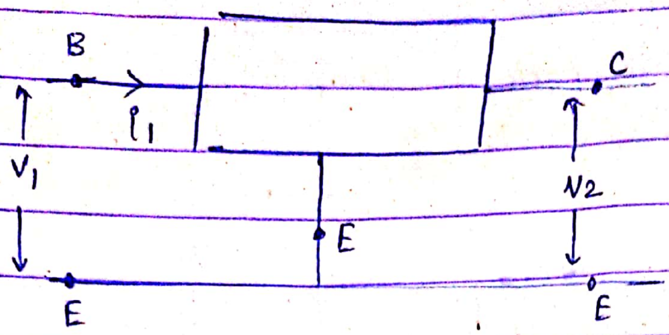


H-parameters or Hybrid parameters: The parameters that relate V_1 & V_2 or the port 1 & port 2.

$$\begin{bmatrix} V_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ V_2 \end{bmatrix}$$

dependent ~~para~~ — independent

$$\boxed{\begin{aligned} V_1 &= h_{11} i_1 + h_{12} V_2 \\ i_2 &= \cancel{h_{21} V_1}\ h_{21} i_1 + h_{22} V_2 \end{aligned}}$$

The dimensions of the parameters $h_{11}, h_{12}, h_{21}, h_{22}$ are hybrid in nature i.e. some of these have dimensions of voltage, some of current & some might be dimensionless.

Generally i_b is fixed i.e. independent and ∵ $i_c = \beta i_b$, i_c is dependent variable.

Input voltage V_1 is dependent because output voltage affects the input voltage when it feeds back to the input side.

when output port is short circuited :

$$r_i \equiv h_{11} = \frac{V_1}{i_1}\bigg|_{V_2=0}$$

short-circuit input impedance. (unit = Ω)

$$\beta \equiv h_{21} = \frac{i_2}{i_1}\bigg|_{V_2=0.} \quad \text{(dimensionless)}$$

forward current gain

when input port is open circuit;

reverse voltage gain

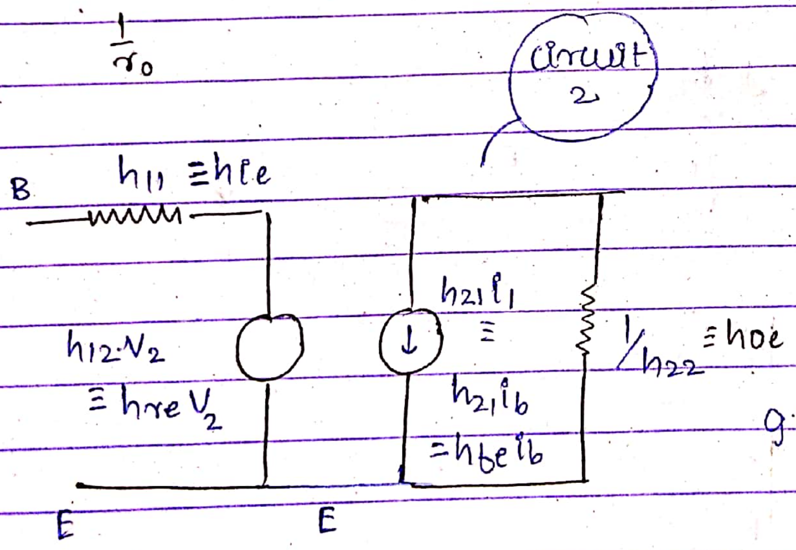
$$\frac{V_1}{V_2} = h_{12}\bigg|_{i_1=0.} \quad \text{(unit : dimensionless)}$$

$\boxed{V_1 = h_{12} V_2}$

feeded back to

$$h_{22} = \frac{i_2}{V_2}\bigg|_{i_1=0.} \quad \text{(unit : siemens)}$$

$\equiv \frac{1}{r_0}$



$h_{ie} = h_{11}$ = input current for common emitter.

h_{re} = reverse voltage gain due in common emitter

Transistor equivalent circuit in terms of hybrid parameters

$$\begin{bmatrix} V_{be} \\ i_c \end{bmatrix} = \begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} \begin{bmatrix} i_b \\ V_{ce} \end{bmatrix}$$

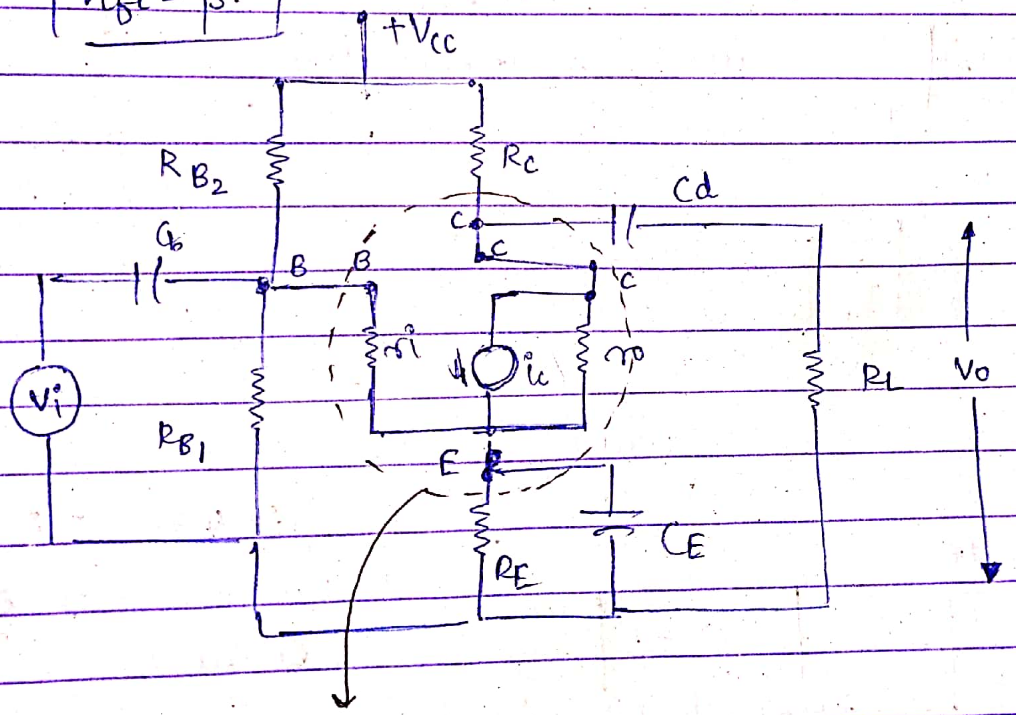
#

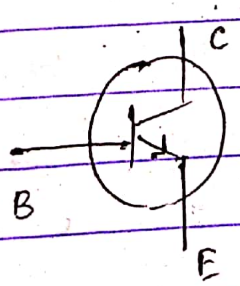
The values of 'h_{re}' are very small. Therefore, it is neglected.

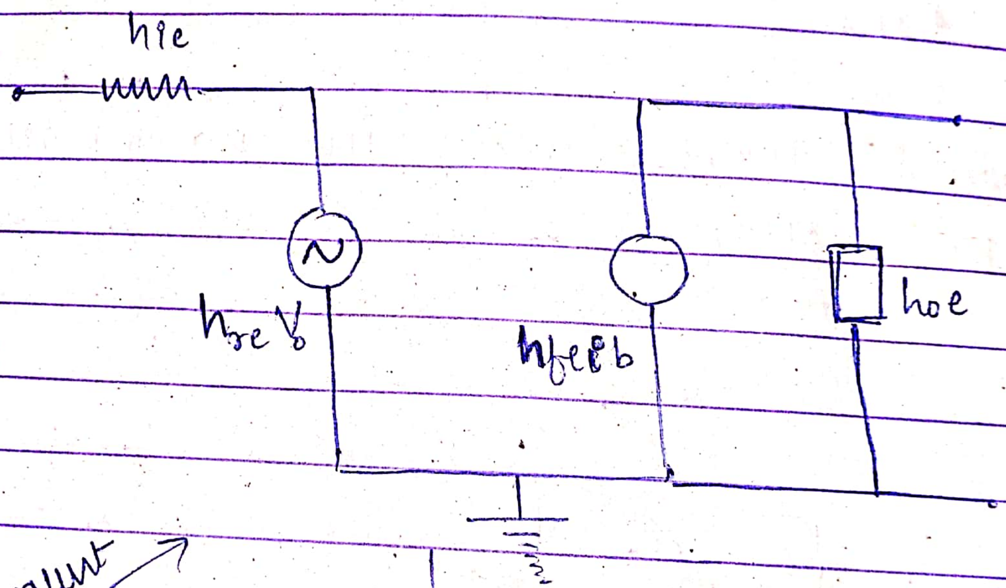
$$\boxed{\begin{matrix} V_1 \equiv V_{BE} \\ V_2 \equiv V_{CE} \end{matrix}}$$

On comparing the circuits 1 & 2,

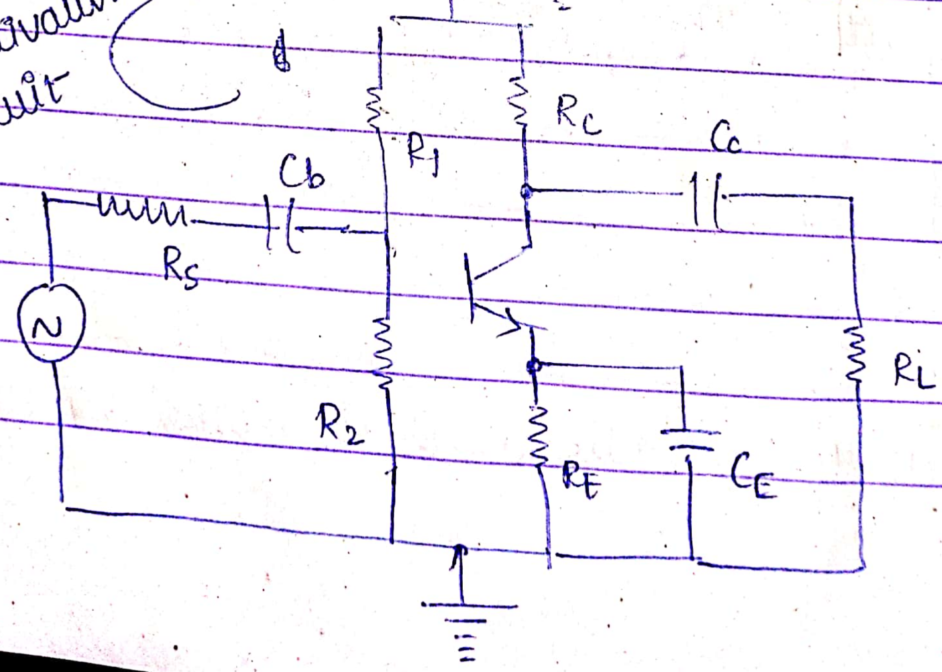
$\boxed{h_{fe} = \beta.}$





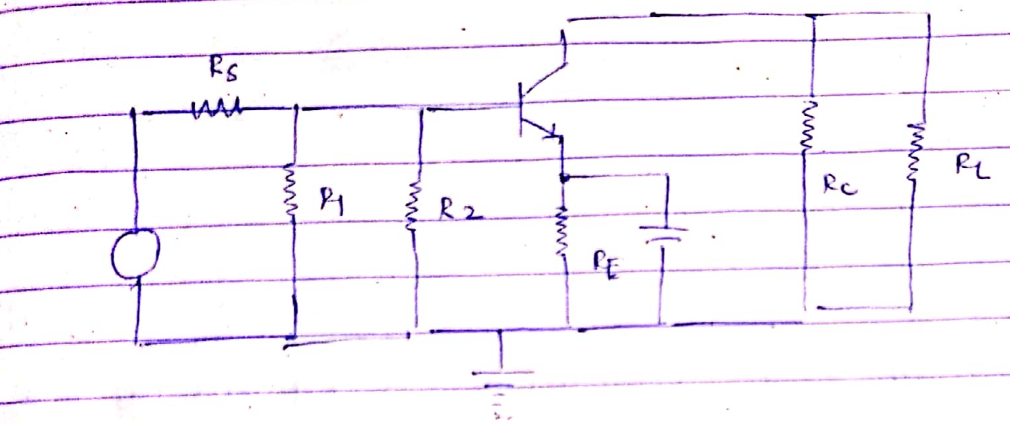


AC equivalent circuit



because capacitors provide low reactance path to 'ac'

All capacitors are considered short-circuited & 'dc' sources also short-circuited.



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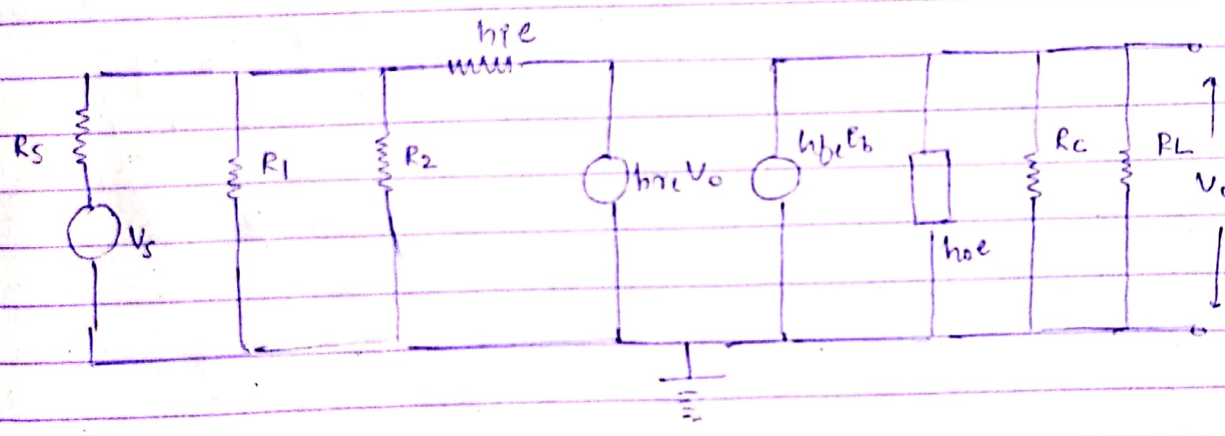

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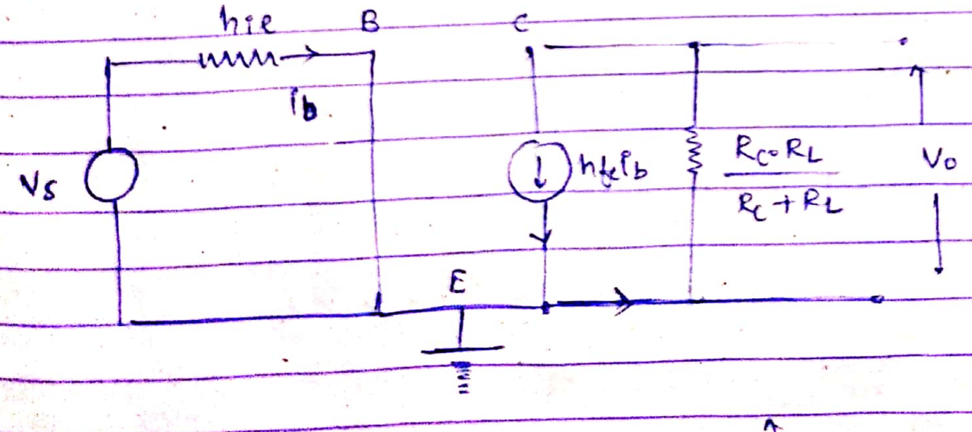


After approximation

Approximations:
- Resistance of an ideal voltage source = 0
- R_1 & R_2 will not affect i_B.
- h_{oe} can be neglected, ∵ it is in parallel.

$V_o = -(h_{fe} \cdot i_b) \cdot R_o$

$$\boxed{V_o = -h_{fe}\, i_b \left(\frac{R_C R_L}{R_C + R_L}\right)}$$

indicates phase difference of 180° between input & output

current ga voltage gain $= \frac{V_o}{V_i}$

$$= \frac{-h_{fe} \cdot \cancel{i_b} \cdot \left(\frac{R_C R_L}{R_C + R_L}\right)}{\cancel{V_i} \cdot h_{ie}\, \cancel{i_b}}$$

* voltage gain $= \frac{-h_{fe}}{h_{ie}} \left(\frac{R_C R_L}{R_C + R_L}\right)$

* Input impedance $= h_{ie}$

* output impedance $= R_o$.

* current gain $= \frac{i_o}{i_{in}}$

$$= \frac{h_{fe} \cancel{i_b}}{\cancel{i_b}} = h_{fe}.$$

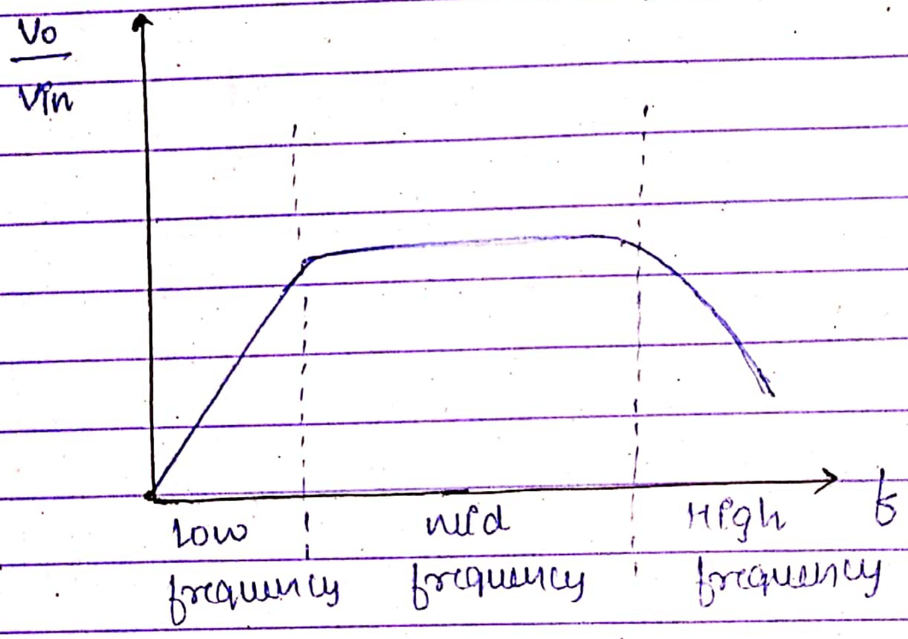
* Power gain $= V_{gain} \times I_{gain}$

$$= \frac{-h_{fe}}{h_{ie}} \cdot R_o \cdot h_{fe} = \frac{-h_{fe}^2}{h_{ie}} \cdot R_o.$$

Frequency Response:

Gain or Magnitude vs frequency
$\left(\frac{V_o}{V_{in}}\right)$

lower cut-off frequency is decided by the 'RC' network due to the capacitor we neglected (C_b). $\left\{ f_c = \frac{1}{2\pi R_1 C} \right\}$



unipolar i.e. only one carrier (majority charge carrier) takes part in conduction.

~~Junction~~ (Field Effect Transistor)

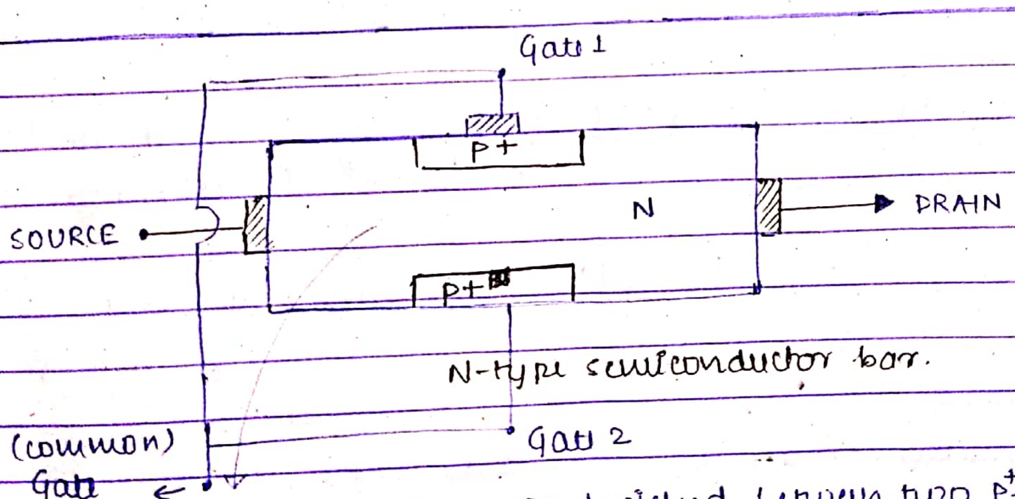
JFET
Junction Field Effect transistor.

MOSFET / IGFET
Metal oxide semiconductor / Insulated Gate Field Effect Transistor

BJT is a current controlled device, ~~unlike FET which is a unipolar device.~~

FET is a unipolar device.

BJT	FET
→ Bipolar device	→ unipolar device
→ current controlled device	→ voltage controlled device
→ Input impedance is very low.	→ Input impedance is very High.
→ output will be noisy (or) due to both the charge carriers	→ output



channel is the portion sandwiched between two P^+ layers

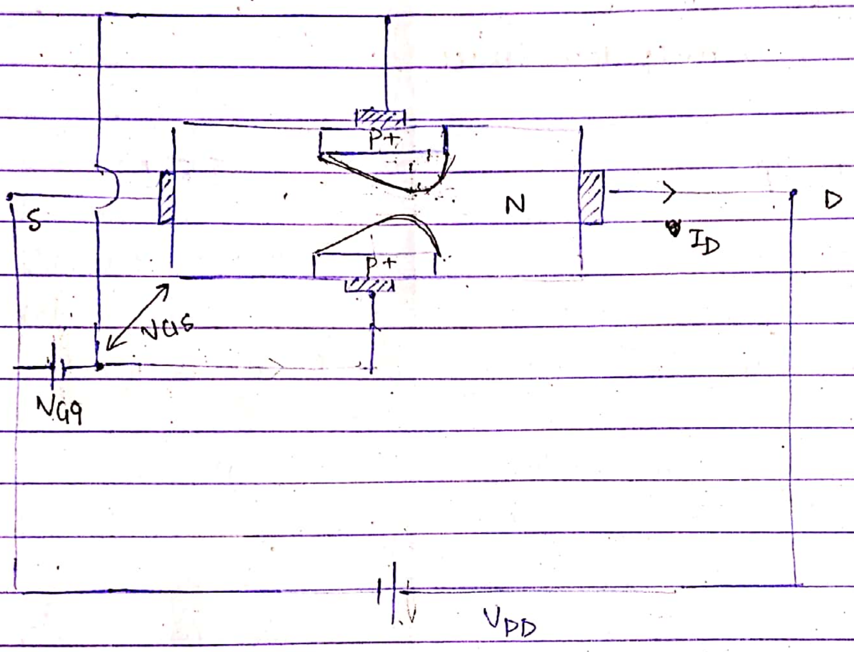
on applying certain voltage at the common gate, an electric field is created at the junction of P^+ layers & N-channel. Thus, the transistor's name is Junction field Effect transistor.

The figure shown is of N-channel FET.

source & ~~terminal~~ drain terminals can be interchanged.

It is voltage controlled because voltage applied at the common gate is what controls the flow of majority carriers.

The voltage (V_{GS}) at which the



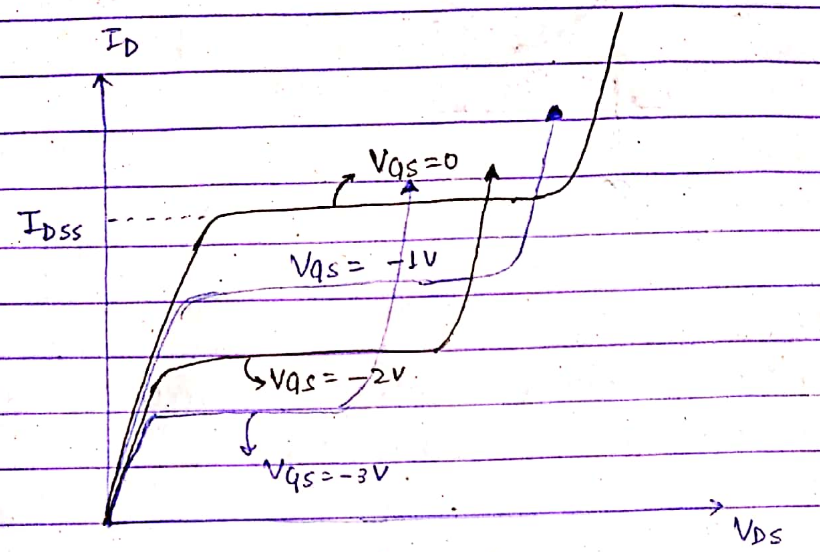
$I_D = f\,\cancel{I_D}(V_{GS}, V_{DS})$

$I_D = f(V_{DS})\big|_{V_{GS} = \text{constant}}$: output characteristic.

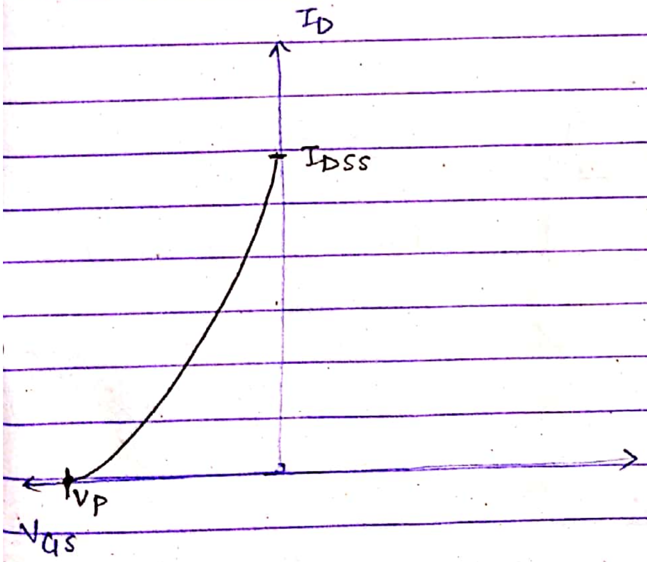
$I_D = f(V_{GS})\big|_{V_{DS} = \text{constant}}$: Transfer characteristic

The channel 'N' acts as a resistance. Since resistance $\propto$ length, ∴ voltage drop near the drain side is maximum. Thus, width of depletion layer varies

The depletion layer touches at certain value of V_{GS}. This voltage is called <u>pinch-off voltage</u>. After this a constant current flows. Thus on increasing V_{DS}, it reaches the zener breakdown stage & current hikes up suddenly.

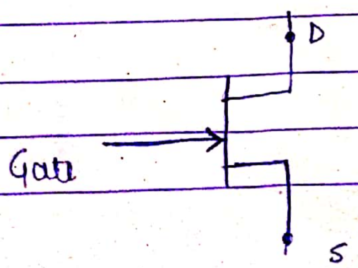


output characteristics



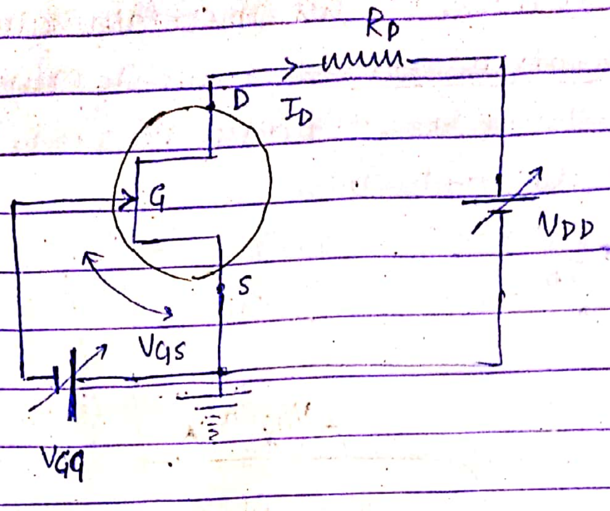
Transfer characteristics

<u>Symbol:</u>



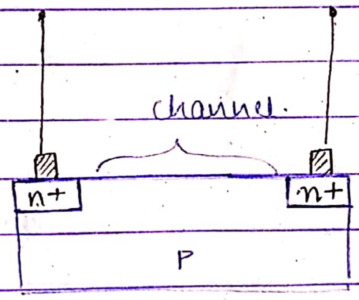
convention:

when P-N junction is forward biased, current flows towards the gate.

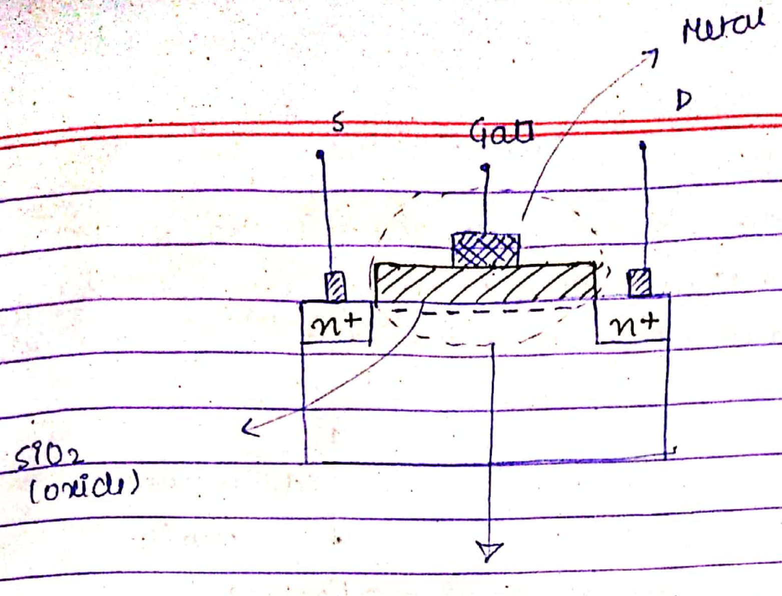


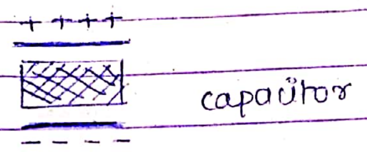
MOSFET:

The semiconductor taken is called substrate. To make an N-type MOSFET, we take P-type substrate.



A layer of SiO_2 acts as an insulator to behave ~~as~~ analogous to the dielectric in a capacitor. This is done to attain capacitive action.



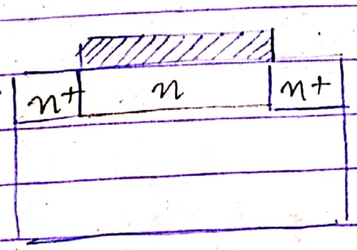


Recombination at the semiconductor plate is less because the charge increases of holes are not too much in no.

MOSFET

- Enhancement type
- Depletion type.

- The Gate to source voltage at which the channel gets inverted is called Threshold voltage.



Depletion type MOSFET can be used in both the modes:

(i) Enhancement

(ii) Depletion.

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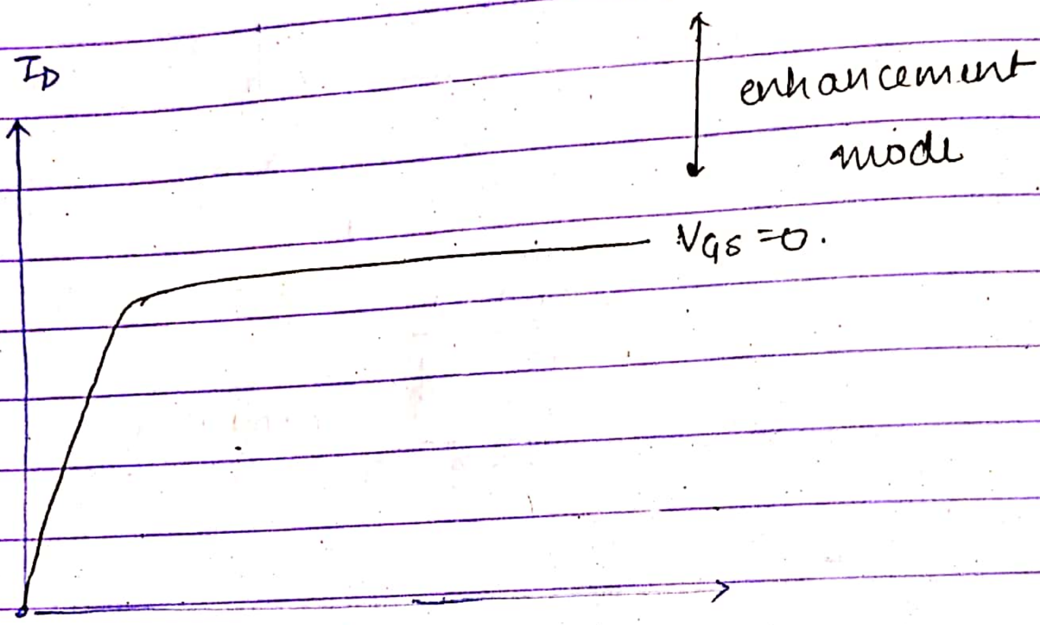
(i)

When V_{GS} is positive & is increased, negative charges appear at the semiconductor plate & there is an increase in no. of electrons. Thus, current increases and it acts ~~as~~ in enhancement mode.



(ii)

Similarly when V_{GS} is -ve, positive charge appears at the semiconductor plate & no. of electrons reduces thus reducing the drain current.