EC102: ELECTRONICS & COMMUNICATION LABORATORY

LIST OF EXPERIMENTS:

1. Measurement of voltage, time period and frequency of different signals on CRO. Measurement of frequency and phase of two different signals using Lissajous pattern.
2. To determine the forward and reverse bias characteristics of PN junction diode.
3. To determine the reverse bias characteristics of Zener diode and its application as a voltage regulator.
4. Measurement of rectification efficiency and ripple factor of Half-wave and Full-wave rectifier circuits with and without C-Filter.
5. To determine the frequency response of CE transistor amplifier and finding its gain Bandwidth product.
6. To determine the output and transfer characteristics of JFET and measurement of its voltage gain.
7. Design of RC phase shift oscillator using IC-741 Op-Amp and finding its frequency of oscillation.
8. Design of Inverting and Non-inverting amplifier using IC 741 OP-AMP and finding its frequency response.
9. Realization of Basic logic gates (AND, OR, NOT) using NAND Gate (IC-7400).
10. Implementation of Boolean expression F = (A.B.C + D.E) using AND Gate(IC 7408) and OR Gate (IC 7432).
11. Generation of Amplitude modulated wave and calculation of percentage of modulation using standard setup.
12. Generation of FM-wave and its detection using standard setup.

Text Books:

1. Millman J., Halkias C.C., Parikh Chetan, "Integrated Electronics: Analog and Digital Circuits and Systems", Tata McGraw-Hill, 2/e.
2. Mano M.M., "Digital Logic and Computer Design", Pearson Education, Inc, Thirteenth Impression, 2011.
3. Singal T. L., "Analog and Digital Communications", Tata McGraw-Hill, 2/e.
4. Haykin S., Moher M., "Introduction to Analog & Digital Communications", Wiley India Pvt. Ltd., 2/e.

Reference Book:

1. Boylstead R.L., Nashelsky L., "Electronic Devices and Circuit Theory", Pearson Education, Inc, 10/e.

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

EC102: ELECTRONICS & COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

EXPERIMENT NO - 1

MEASUREMENT OF VOLTAGE, TIME PERIOD AND FREQUENCY OF DIFFERENT SIGNALS ON CRO. MEASUREMENT OF FREQUENCY AND PHASE OF TWO DIFFERENT SIGNALS USING LISSAJOUS PATTERN.

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM (A): Measurement of the following using Cathode Ray Oscilloscope (CRO):

a. DC Voltage
b. Peak & RMS Value of AC Voltage
c. Time Period and Frequency of Periodic Signals (Sine wave, Square wave, Triangular wave)

APPARATUS REQUIRED:

1. Power Supply
2. CRO
3. Function Generator

THEORY:

Cathode ray oscilloscope is one of the most useful electronic equipment, which gives a visual representation of electrical quantities, such as voltage and current waveforms in an electrical circuit. It utilizes the properties of cathode rays of being deflected by an electric and magnetic fields and of producing scintillations on a fluorescent screen. Since the inertia of cathode rays is very small, they are able to follow the alterations of very high frequency fields and thus electron beam serves as a practically inertia less pointer. When a varying potential difference is established across two plates between which the beam is passing, it is deflected and moves in accordance with the variation of potential difference. When this electron beam impinges upon a fluorescent screen, a bright luminous spot is produced there which shows and follows faithfully the variation of potential difference. From the trace of the signal several measurements can be made.

Measurement of DC Voltage: Deflection on a CRO screen is directly proportional to the voltage applied to the deflecting plates. Therefore, if the screen is first calibrated in terms of known voltage. i.e. the deflection sensitivity is determined, the direct voltage can be measured by applying it between a pair of deflecting plates. The amount of deflection so produced multiplied by the deflection sensitivity, gives the value of direct voltage.

V = (No. of Divisions) x (Volts / Division)

Measurement of AC voltage: To measure the alternating voltage of sinusoidal waveform, The A.C. signal, from the signal generator, is applied across the y – plates. The voltage (deflection) sensitivity band switch (Y-Plates) and time base band switch (X-Plates) are adjusted such that a steady picture of the waveform is obtained on the screen. The vertical height (l) i.e. peak-to-peak height is measured. When this peak-to-peak height (l) is multiplied by the voltage (deflection) sensitivity (n) i.e. volt/div, we get the peak-to-peak voltage (2Vp). From this we get the peak voltage (Vp). The rms voltage Vrms is equal to $V_P/\sqrt{2}$. This rms voltage Vrms is verified with rms voltage value, measured by the multi-meter.

Measurement of Frequency: An unknown frequency source (signal generator) is connected to y- plates of C.R.O. Time base signal is connected to x – plates (internally connected). We get a sinusoidal wave on the screen, after the adjustment of voltage sensitivity band switch (Y-plates) and time base band switch (X-plates). To calculate the frequency of the observed signal, one has to measure the period, i.e. the time taken for 1 complete cycle, using the calibrated sweep scale.

The period could be calculated by:

T = (No. of Divisions) x (Time / Division)

Once the period T is known, the frequency is given by:

f (Hz)= 1/T(sec)

PROCEDURE:

For DC Voltage measurement

1. Connect the CRO probes to the output of function generator.
2. Keep frequency of the function generator at zero and amplitude to any value.
3. Get the DC voltage by CRO.

For AC Voltage & Frequency measurement:

1. Connect the CRO probes to the output of function generator.
2. Observe the peak values (V_p) of the wave currently selected.
3. Calculate the RMS value of the ac signal by the given formula $V_{rms} = (V_p / \sqrt{2})$.
4. Observe the Time-Period (T) of the wave selected.
5. Calculate the frequency by f = 1/T.
6. Change the both voltage and time period scale and repeat the step 2 to step 5 for three different readings.
7. Take another waveform (sine/square/triangular) and repeat step 2 to step 6.

OBSERVATIONS:

For DC Voltage:

1. From Function generator: Input frequency = 0 Hz;

2. From CRO:

Scale on Volts/div (Volts) = …….
No of div. for Voltage = …….
DC voltage = ……..

For Sine wave measurements:

1. From Function generator:
   Input voltage: ……. volts; Input frequency = ……Hz;
2. From CRO:

Sl. No.	Scale on Volts/ div (V)	Scale on Time/ div (sec)	No of div. for Peak Voltage V_p	No of div. for Time-Period T	Peak voltage V_p (V)	Rms Voltage $V_{rms} = V_p/\sqrt{2}$ (V)	Time Period T (sec)	Measured Frequency f (Hz)
1								
2								
3								

For Square wave measurements:

1. From Function generator:
   Input voltage: ……. volts; Input frequency = ……Hz;
2. From CRO:

Sl. No.	Scale on Volts/ div (V)	Scale on Time/ div (sec)	No of div. for Peak Voltage V_p	No of div. for Time-Period T	Peak voltage V_p (V)	Rms Voltage $V_{rms} = V_p/2$ (V)	Time Period T (sec)	Measured Frequency f (Hz)
1								
2								
3								

For Triangular wave measurements:

1. From Function generator:
   Input voltage: …….. volts; Input frequency = …….Hz;
2. From CRO:

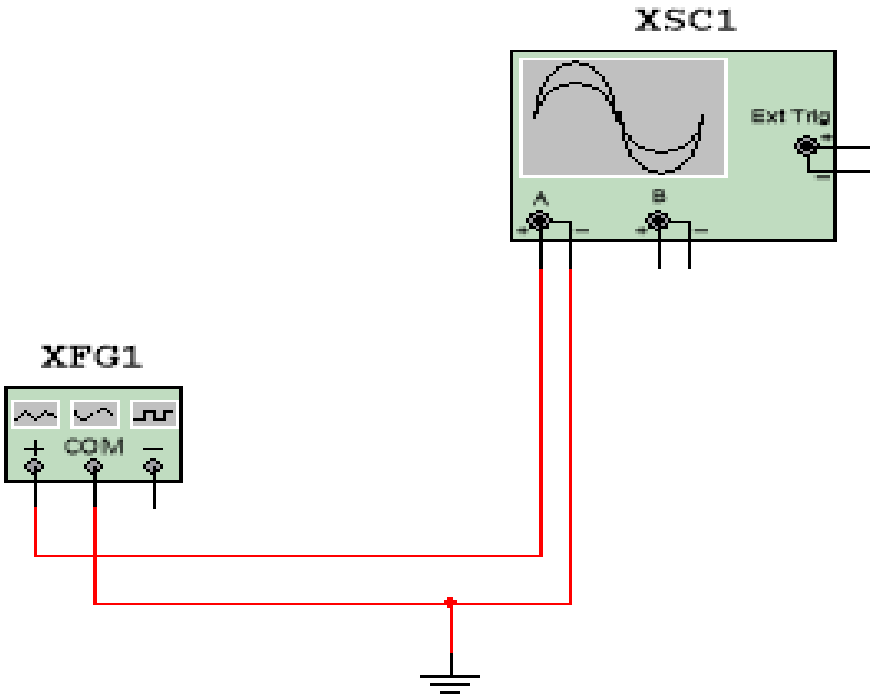
Sl. No.	Scale on Volts/ div (V)	Scale on Time/ div (sec)	No of div. for Peak Voltage V_p	No of div. for Time-Period T	Peak voltage V_p (V)	Rms Voltage $V_{rms} = V_p/\sqrt{3}$ (V)	Time Period T (sec)	Measured Frequency f (Hz)
1								
2								
3								

RESULT & DISCUSSION:

PRECAUTIONS:

1. The continuity of the connecting wires should be tested first.
2. The frequency of the signal generator should be varied such that steady wave form is formed.
3. Readings should be taken carefully.

EXPERIMENTAL SETUP:



(Circuit diagram for the measurement voltage, time period and frequency)

AIM (B): Measurement of unknown frequencies using Lissajous pattern.

APPARATUS REQUIRED:

1. Power Supply
2. CRO.
3. Function Generator (Two)

THEORY:

Two super-position of the two harmonic functions such as sine wave produce a Lissajous Pattern on the CRO screen. Lissajous pattern may be a straight line, an ellipse or a circle depending on the frequency, phase and amplitude of the two signals.

A straight line results when the two waves are in phase or exactly 180˚ out of phase with each other. A circle is displayed when the phase difference is 90˚ and the signals are equal in amplitude.

If f_y corresponds to the frequency of vertical deflection voltage and f_x corresponds to the horizontal deflection voltage then,

f_y / f_x = No. of horizontal tangencies (HT) / No. of vertical tangencies (VT)

Where,

Horizontal Tangency (HT): It is the no of times, a factitious straight line taken at any one Horizontal side of the Lissajous pattern (Up/Down) serves as a tangent to the Lissajous pattern.

Vertical Tangency (VT) is the no of times, a factitious straight line taken at any one Vertical side of the Lissajous pattern (Up/Down) serves as a tangent to the Lissajous pattern.

Hence f_y can be found if f_x is known.

PROCEDURE:

1. An oscillator of unknown frequency is connected to the vertical plate of the CRO and standard oscillator of known frequency is connected to horizontal plate.
2. Adjust the voltage of the two oscillators to give a pattern of a suitable size.
3. Vary slightly the frequency of the test oscillator until a simple Lissajous pattern is obtained. Read known frequency f_x.
4. Find HT and VT from Lissajous Pattern.
5. Calculate f_y by the given formula.
6. Repeat the step 3 and 4 and take five different readings.

OBSERVATIONS:

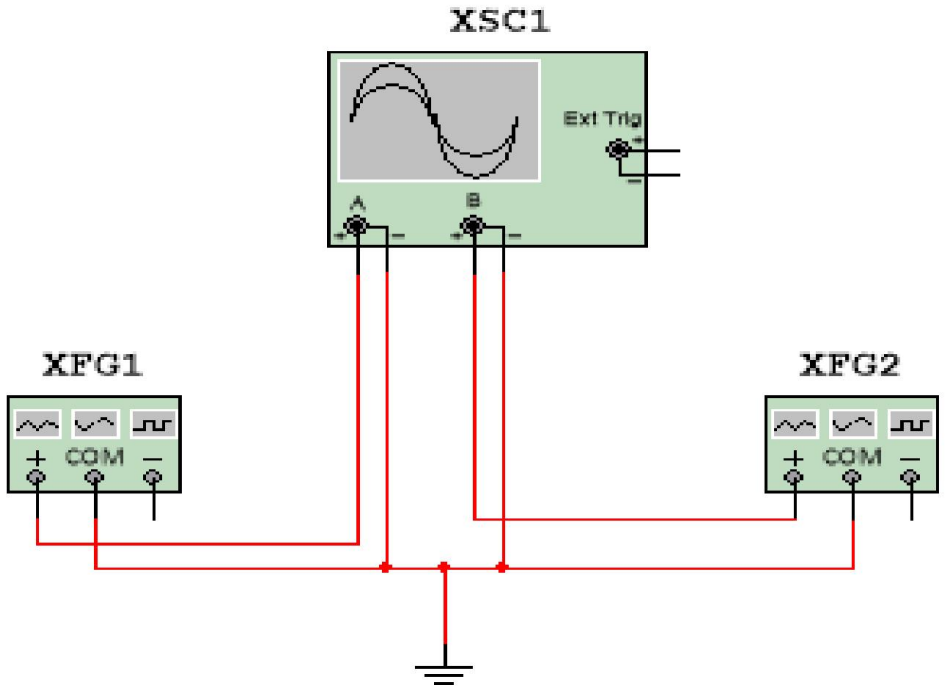
Sl. No.	f_X (Hz)	Horizontal Tangency (HT)	Vertical Tangency (VT)	$f_Y = \frac{HT}{VT} \cdot f_X$ (Hz)
1.				
2.				
3.				
4.				
5.				

RESULT & DISCUSSION:

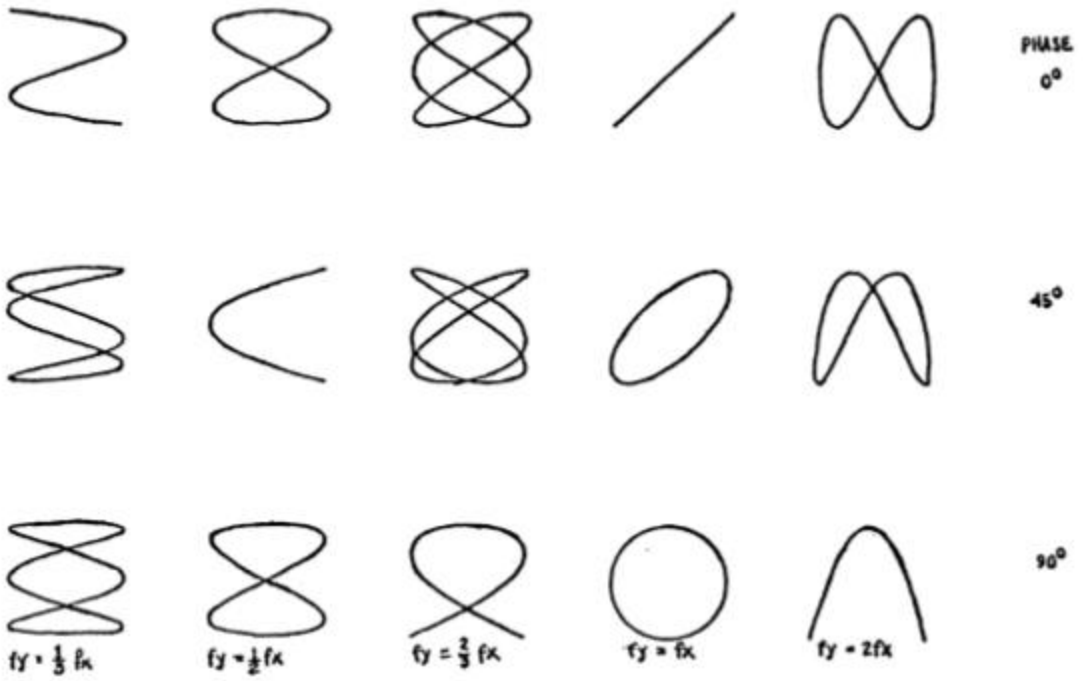
PRECAUTIONS:

1. The continuity of the connecting wires should be tested first.
2. The frequency of the signal generator should be varied such that steady wave form is formed.
3. Readings should be taken carefully.

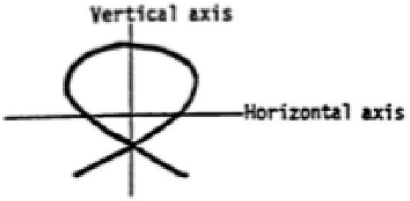
EXPERIMENTAL SETUP:



(Circuit diagram for the Measurement of unknown frequencies using Lissajous pattern)



Sine-vs-sine plots (Lissajous figures) for several frequency ratios



For example, the frequency ratio would be:

$$\frac{f_y}{f_x} = \frac{\text{number of horizontal crossings}}{\text{number of vertical crossings}} = \frac{2}{3}$$

Thus,

$$f_y = 2/3\, f_x\,.$$

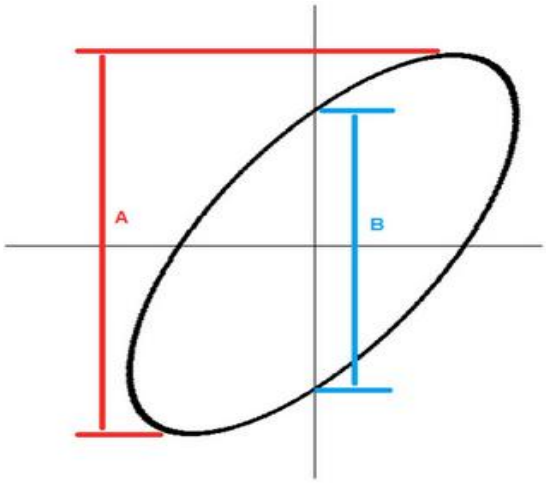
AIM (C): Measurement of phase angle between two signals of same frequency using CRO.

APPARATUS REQUIRED:

1. Power Supply
2. CRO
3. Function Generator
4. RC Network

THEORY:

When two Sinusoidal signals of different amplitudes and equal frequencies are applied to Y-input and X-input of the CRO an ellipse is obtained.



$$\sin \Phi = \frac{B}{A}$$

Φ = Phase Angle

PROCEDURE:

1. Observe and trace the Ellipse on tracing paper and Measure Y intercept and Y peak
2. Note down the frequency of wave applied from Function Generator.
3. Calculate the phase difference as;

Theoretical $\phi = \tan^{-1}(\omega RC)$

Experimental $\phi = \sin^{-1}$ [Y-intercept (B) / Y-peak (A)]

OBSERVATIONS:

R = 3.9 KΩ; C = 33 nF

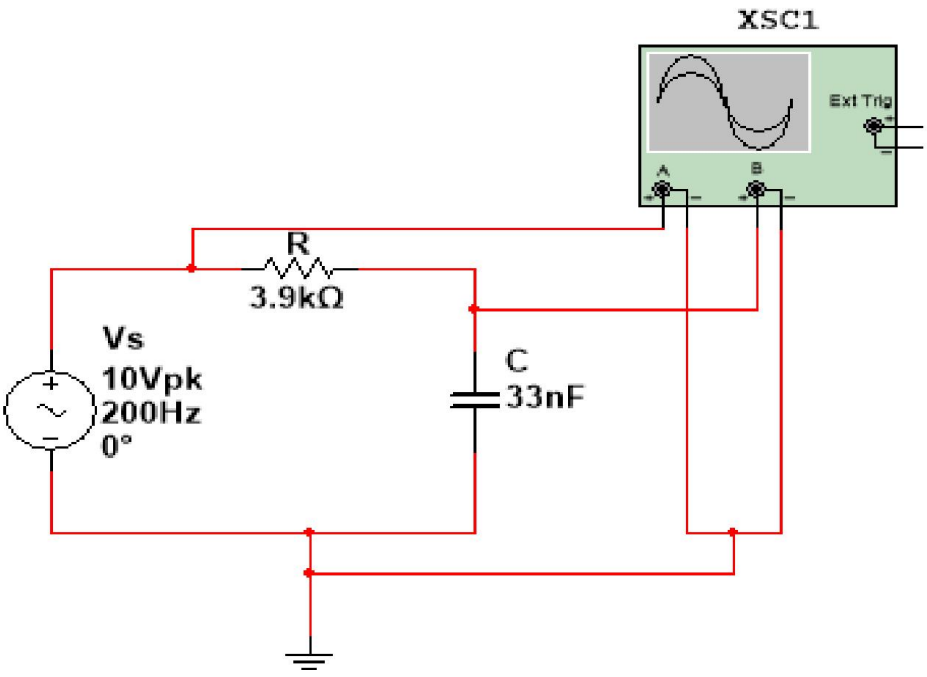
Frequency of applied signal (Hz)	(θ_1) $\phi=\tan^{-1}\omega RC$	(B) Y-intercept	(A) Y-peak	(θ_2) Sin^{-1} (B/A)	Error (θ_1- θ_2)
100					
500					
1000					
1500					
2000					

RESULT & DISCUSSION:

PRECAUTIONS:

1. The continuity of the connecting wires should be tested first.
2. The frequency of the signal generator should be varied such that steady wave form is formed.
3. Readings should be taken carefully.

EXPERIMENTAL SETUP:



(Circuit diagram for the measurement of phase angle)

APPENDIX

CRO FRONT PANEL CONTROL & THEIR FUNCTIONS

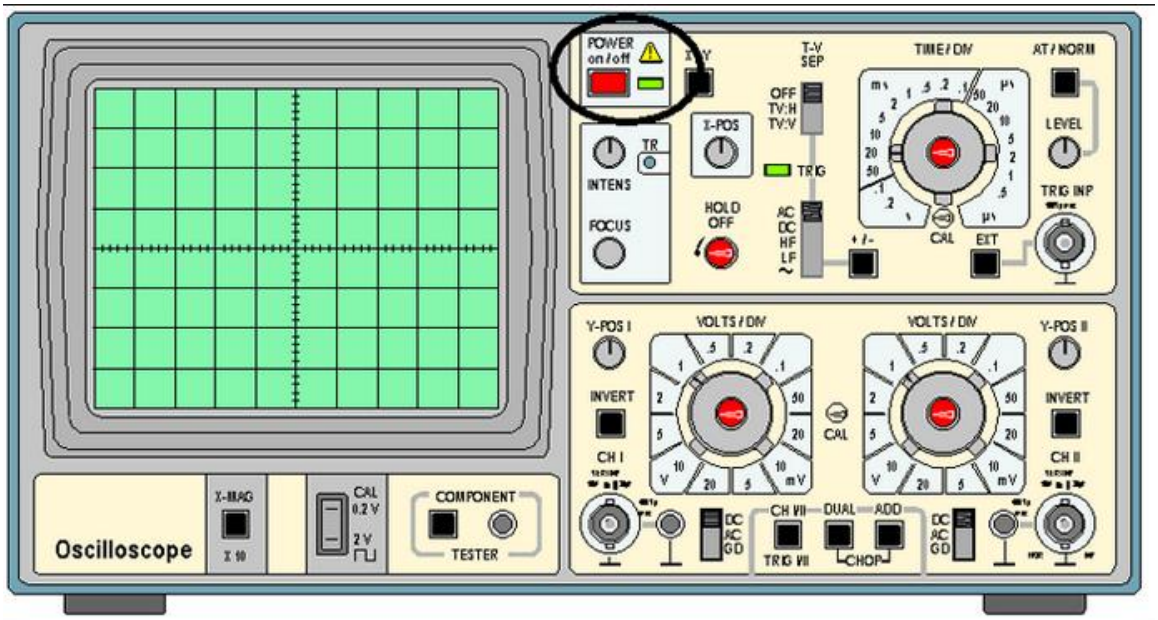


Fig. Front Panel of CRO

1.	POWER ON	Put the instrument to main supply with LED indication.
2.	INTENSITY	Controls the brightness of the display.
3.	FOCUS	Controls the sharpness of the display
4.	TIME BASE	18 step switch to enable selection of 18 calibrated sweep from 0.5 micro sec/div to0.2s/div in 1,2,5,….sequence
5.	TIME BASE VARIABLE	In calibrated position(CAL)the selected sweep speed holds indicated calibration clockwise. It extends the sweep speed by 2.5 times approx. with the LED indication.
6.	HOLD-OFF	Provides 4:1 Hold off to enhance HF &Complex Signal Triggering.
7.	⇔ POSITION/x5	Controls the horizontal position of the display. When this control is pulled, it magnifies the sweep 5 times with LED indication.
8.	LEVEL	Variable control, selects the trigger point on the displayed waveform.
9.	AUTO/NORM	In auto mode trace is displayed in absence of any input signal. The display is then automatically triggered for signals above 30 Hz depending upon correct setting of trigger LEVEL controls.

10.	INT/EXT	INT; Display triggers from signals derived from CH1, CH2 or line.EXT: triggering from any other external source fed through EXT TRIG BNC socket.
11.	LINE	Triggers from power line frequency.
12.	TV	Triggers from low freq. component of TV signal (TV-V or TV-H).
13.	+/-	Selects trigger point on either positive or negative slope of the displayed waveform.
14.	CH1/CH2	Select trigger signal in INT mode derived from either CH1 or CH2 inputs.
15.	HF Rej	Introduces low pass filter (20 KHz) in trigger.
16.	ac/dc	Selects trigger signal coupling.
17.	SWP/X-Y	When pressed, converts CH2 input into x-channel and enable use of the scope as on X-Y scope (Y-input via. CH1). In released position, SWEEP operates.
18.	0.2, 1KHz	200 mv p-p 1 KHz square wave calibration signal.
19.	⇳ Positions	Controls the vertical position of the display
20.	ac/dc/gnd	Selects input coupling / grounding (Grounds the amplifier input but input signal is open circuited)
21.	EXT-TRIG	Input BNC for external trigger signal
22.	INPUT BNC CH1/Y (CH2/X)	Input terminals to CH1/Y, CH2/X inputs
23.	TRACE	Screw driver control to adjust horizontal tilt of the trace.
24.	CH1/CH2 ATTENUATOR	12 steps compensated attenuator from 5 mv/div to 20 V/div in 1,2,5 sequence.
25.	VERTICAL MODES	
	a. ALT/CHOP	Selects switching mode for 2 channel while in DUAL operations
	b. DUAL/MONO (X-Y)	In DUAL, operates as a DUAL trace scope in ALT or CHOP mode as selected.
	c. CHANNEL ADDTION (CH1-CH2)	In DUAL mode, when ADD switch is pressed signals of CH1 and CH2 are algebraically added.
	d. CHANNEL SUBRACTION (CH1-CH2)	In DUAL mode, when ADD and CH2 INV switches are pressed CH2 signal is algebraically subtracted from CH1 signal.
	e. CH2 INV	When CH2 INV switch is pressed polarity of the signal to CH2 is inverted.

FIRST TIME OPERATION: **SET CONTROLS AS FOLLOWS:**

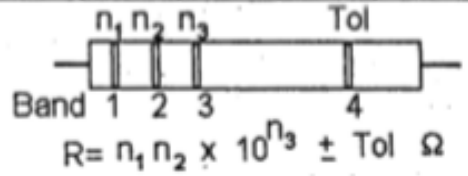
POWER ON	: Switch In OFF position
INTENSITY	: Mid position
FOCUS	: Mid position
ATTENUATOR CH1/CH2	: 50 mv/div
VERTICAL SHIFT CH1/CH2	: Mid position
dc/ac	: dc(Release position)
GND	: gnd(Pressed position)
ALT/CHOP	: ALT
DUAL/MONO X-Y	: MONO X-Y
ADD	: released position
CH2 INV	: released position
VARIABLE	: CAL position(fully anticlockwise)
HOLD OFF	: CAL position(fully anticlockwise)
LEVEL	: Mid position
AUTO/NORMAL	: AUTO(Released position)
CH1/CH2	: CH1(Released position)
INT/EXT	: INT (Released position)
+/-	: +(Released position)
ac/dc	: ac(Released position)
TV	: Released position
TV-H/TV-V HF REJ	: Released position
LINE	: Released position
SWP/X-Y	: SWP(Released position)
HORIZONTAL SHIFT	: Mid position
CTC	: Released position

MEASUREMENT OF RESISTANCE, CLASSIFICATION OF CAPACITORS DIODE TESTING

A Note On Reading Resistor Values: The colour bands on resistors are used to indicate the nominal values of their resistance and the permitted tolerance on that value. The first three bands (closest together) give the value of the resistor in ohms (Ω). The band at the end of the resistor indicates the first significant digit (n_1) and the next band indicates the second digit (n_2). The third band indicates the number of zeros following these two digits (n_3). The bands are colour coded as follows:

Colour	Black	Brown	Red	Orange	Yellow	Green	Blue	Violet	Grey	White
Digit	0	1	2	3	4	5	6	7	8	9

A red fourth band means the resistor's value will be within 2% of the stated value, gold 5%, and silver 10%, Absence of the fourth band indicates a ±20% tolerance.



A Note On Reading Capacitor Values: ***Big capacitors*** **are polarized. The terminal - (+) must be at least as negative (positive) as the other terminal. These have values marked in μF.**

Smaller Capacitors: Tantalum: These are often coloured cylinders. Mylar: These are yellow cylinders made of long coils of metal foils separated by thin dielectrics. Fat rectangular shaped capacitors are often made of Metallized Polyster film. Ceramic: These are often disc shaped.

While reading small capacitor values one must remember that in electronics these are in the range pF- μF (a few pF to a few μF). Some examples of the markings and the corresponding values are given below.

Markings	A100	10KH	475K	475M	.01M	.1MFD	473J
Read as	100pF ±20%	10 KpF ±20%	47×10^5pF ±10%	47×10^5pF ±20%	.01μF ±20%	0.1μF ±20%	0.047μF ±5%
Markings	4R7μ	560M	101K	4k7	22n	0.1	Colour band
Read as	4.7μF ±20%	560pF ±20%	10×10^1pF ±10%	4.7×10^3pF ±20%	22nF ±20%	0.1μF ±20%	Value read from top to bottom.

ADDITIONAL NOTE ON READING CAPACITOR VALUES:

Large capacitors have the value printed plainly on them, such as 10μF (Ten Micro Farads) but smaller disk types along with plastic film types often have just 2 or three numbers on them?

First, most will have three numbers, but sometimes there are just two numbers. These are read as Pico-Farads. An example: 47 printed on a small disk can be assumed to be 47 Pico-Farads (or 47 puff as some like to say)

Now, what about the three numbers? It is somewhat similar to the resistor code. The first two are the 1st and 2nd significant digits and the third is a multiplier code. Most of the time the last digit tells you how many zeros to write after the first two digits, but the standard has a couple of curves that you probably will never see. But just to be complete here it is in a table.

Third digit	Multiplier (this times the first two digits gives you the value in Pico-Farads)
0	1
1	10
2	100
3	1,000
4	10,000
5	100,000
6 not used	
7 not used	
8	.01
9	.1

Now for an example: A capacitor marked 104 is 10 with 4 more zeros or 100,000pF which is otherwise referred to as a .1 µF capacitor.

Most kit builders don't need to go further, but I know you want to learn more. Anyway, Just to confuse you some more there is sometimes a tolerance code given by a single letter. I don't know why there were picked in the order they are, except that it kind of follows the middle row of keys on a typewriter.

So a 103J is a 10,000 pF with +/-5% tolerance

Letter symbol	Tolerance of capacitor
D	+/- 0.5 pF
F	+/- 1%
G	+/- 2%
H	+/- 3%
J	+/- 5%
K	+/- 10%
M	+/- 20%
P	+100% ,-0%
Z	+80%, -20%

DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING

EC102: ELECTRONICS & COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

EXPERIMENT NO - 2

TO DETERMINE THE FORWARD AND REVERSE BIAS CHARACTERISTICS OF PN JUNCTION DIODE.

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: To determine the forward and reverse bias characteristics of PN junction diode.

APPARATUS REQUIRED:

1. Power Supply
2. Ammeter
3. Voltmeter

CIRCUIT COMPONENTS:

1. Diodes
2. Resistance (100Ω)
3. Connecting Wires and Breadboard

THEORY:

In a piece of semiconductor material, if one half is doped by P-type impurity and the other half is doped by N-type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. The N-type material has high concentration of free electrons, while P-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over the P-side and holes the N-side. This process is called diffusion. As the free electron moves across the junction from N-type to P-type, the donor irons become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on the P-side of the junction. This net negative charge on the P-side prevents further diffusion of electron in to the P-side. Similarly, the net positive charge on the N-side repels the holes crossing from P-side to N-side. Thus a barrier is set-up near the junction which prevents further movement of charge carriers. As the consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between P and N region, which is called the potential barrier, junction barrier, diffusion potential, or contact potential, V_O. The magnitude of the contact potential V_O varies with doping levels and temperature. V_O is 0.3 V for germanium and 0.72 V for silicon.

FORWARD BIAS

When positive terminal of the battery is connected to the P-type and negative terminal to the N-type of the PN diode, the bias is known as forward bias. Under the forward bias condition, the applied positive potential repels the holes in P-type region so that the holes move towards the junction and the applied negative potential repels the electron in the N-type region and the electron move towards the junction. Eventually, when the applied potential is more than the internal barrier potential the depletion region and internal

potential barrier disappear. A feature worth to be noted in the forward characteristics is the cut in or threshold voltage V_γ below which the current is very small. It is 0.3 V for GE and 0.7 V for Si respectively. At the cut in voltage, the potential is overcome and the current through the junction starts to increase rapidly.

REVERSE BIAS

When the negative terminal of the battery is connected to the P-type and positive terminal of the battery is connected to the N-type of the PN junction, the bias applied is known as reverse bias. Under applied reverse bias, holes which form the majority carriers or the P-side moves towards the negative terminal of the battery and electron which form the majority carrier of the N-side are attracted towards the positive terminal of the battery. Hence, the width of the depletion region which is depleted of the mobile charge carriers increases. Thus the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both the directions. Therefore, theoretically no current should flow in the external circuit. But in practice, a very small current of the order of a few microamperes flows under reverse bias. Electron forming covalent bonds of the semiconductor atoms in the P and N-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. Hence electron-hole pairs are continually produced in both the regions. Under the reverse bias condition, the thermally generated holes in the P-region are attracted towards the negative terminal of the battery and the electrons in the N-region are attracted towards the positive terminal of the battery. Consequently, the minority carriers, electron on the P-region and holes in the N-region, wander over to the junction and flow towards their majority carrier side giving rise to a small reverse current. This current is known as reverse saturation current, I_O. The magnitude of reverse current depends upon the junction temperature because the major source of minority carriers is thermally broken covalent bonds. For large applied reverse bias, the free electrons from the N-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electron from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called as an avalanche of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as breakdown voltage, V_{BD}.

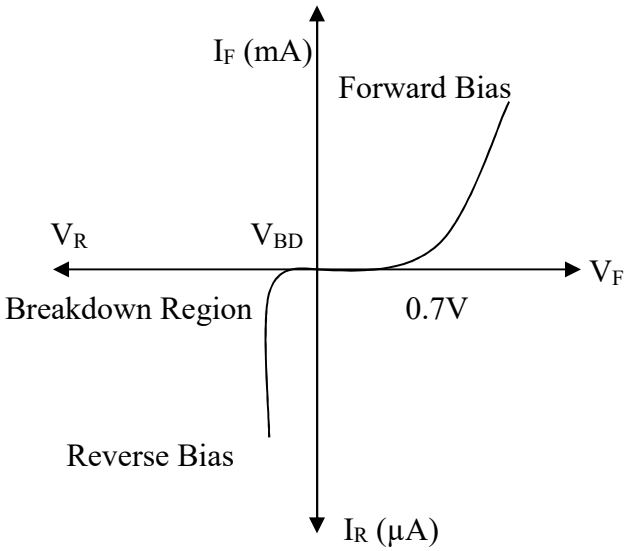
PN DIODE APPLICATIONS

An ideal PN diode is a two terminal polarity sensitive device that has zero resistance when it is forward biased and infinite resistance when it is reverse biased. Due to this characteristic the diode finds number of applications as given below.

1. Rectifier
2. Switch
3. Clamper
4. Clipper
5. Demodulation detector circuits

The graph of voltage applied across the diode (V) versus the current (I) flowing thru it is called its V-I characteristic. A typical V-I characteristic of a p-n junction diode is as shown.

- Static Forward Resistance $R_{dc} = \frac{V_F}{I_F}\ \Omega$
- Dynamic Forward Resistance $r_{ac} = \frac{\Delta V_F}{\Delta I_F}\ \Omega$



PROCEDURE:

1. Connect the circuit as shown in figure 1.
2. Bring the variable voltage of the DC source to zero. The current through milliammeter should also be zero.
3. Increase the variable voltage of the DC source slowly and in steps. Corresponding to each setting, note down the voltmeter and milliammeter readings.
4. Do not exceed the current beyond the current rating of the diode. This completes the observation for V-I characteristics of the forward biased diode.
5. Plot Current (I_F) Voltage (V_F) by choosing proper scales.
6. Make the connections as shown in figure 2.
7. Repeat the steps 2 and 3. This completes observation for V-I characteristics of reverse biased diode.
8. Plot Current (I_R) Voltage (V_R) by choosing proper scales.

OBSERVATIONS:

Table I

Readings for Forward Bias of the diode.

Sl. No.	V_{IN} (volt)	V_F (volt)	I_F (mA)
1.			
2.			
3.			
---	---	---	-----
---	---	-----	-----

Table II

Readings for Reverse bias of the diode.

Sl. No.	V_{IN} (volt)	V_R (volt)	I_R (μA)
1.			
2.			
3.			
---		---	---
---		---	---

RESULT & DISCUSSION:

PRECAUTIONS:

1. The polarities of diodes should be carefully identified.
2. While doing the experiment, do not exceed the ratings of the diode. This may lead to damage the diode.
3. Connect Voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
4. Do not switch-on the power supply unless you have checked the circuit connections as per the circuit diagram.
5. Readings should be taken carefully.
6. Power supply should be switched-off after completion of experiment.

EXPERIMENTAL SETUP:

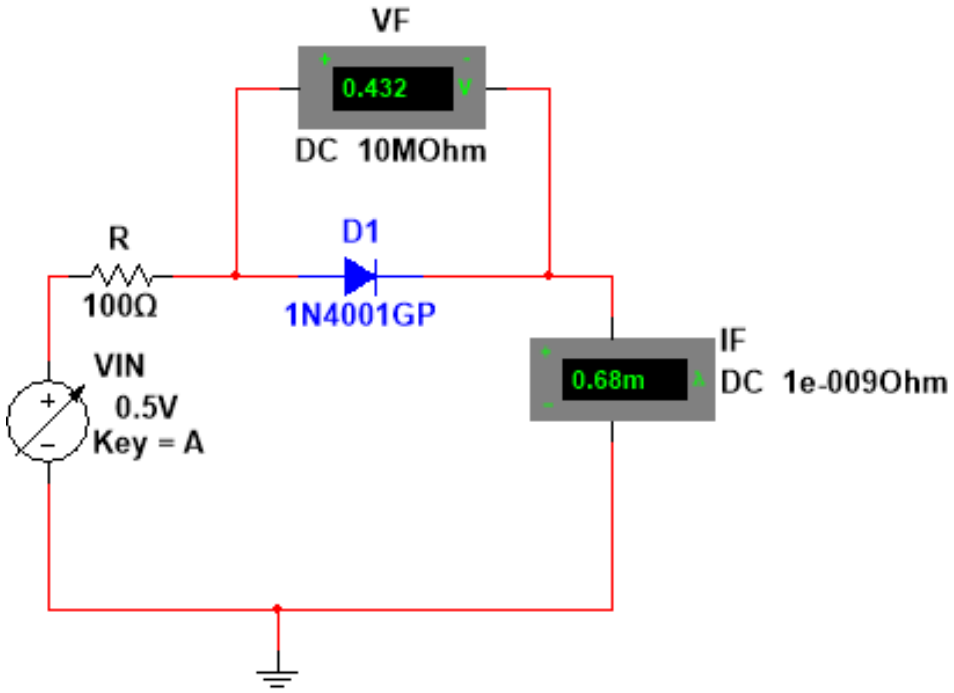


Fig.-1 (Circuit diagram for Forward Biased PN-Diode)

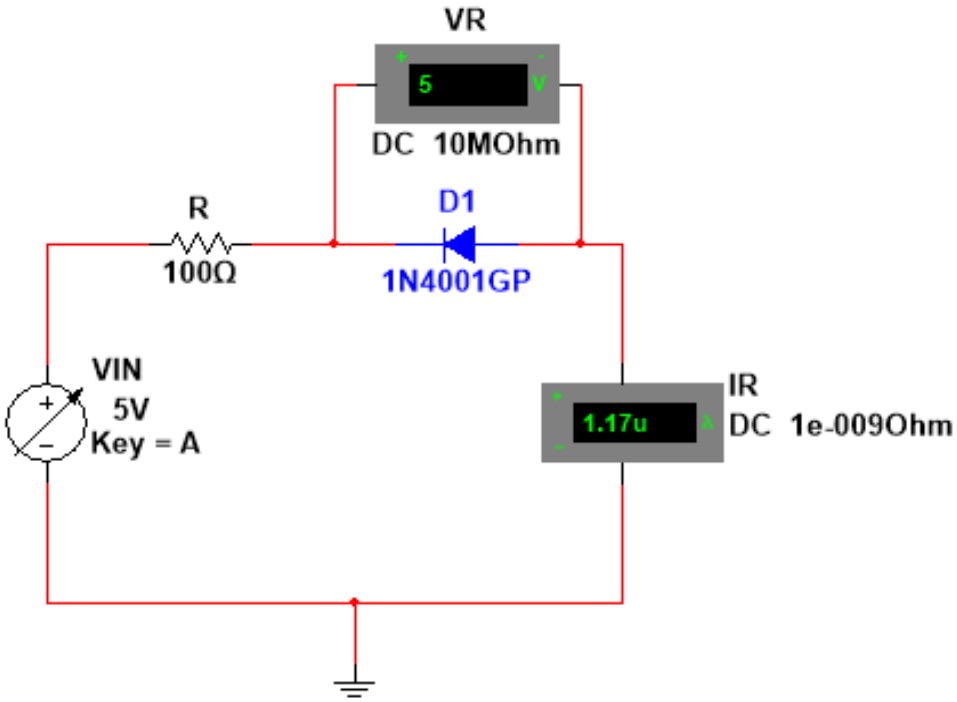


Fig.-2 (Circuit diagram of Reverse Biased PN-Diode)

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EXPERIMENT NO - 3

TO DETERMINE THE REVERSE BIAS CHARACTERISTICS OF ZENER DIODE AND ITS APPLICATION AS A VOLTAGE REGULATOR.

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: To determine the reverse bias characteristics of Zener diode and application as a voltage regulator.

APPARATUS REQUIRED:

1. Power Supply
2. DC Voltmeter
3. DC Ammeter

CIRCUIT COMPONENTS:

1. Resistor 470Ω, 1.5K, 2.2K, 3.3K, 5.6K, 12K
2. Zener EC 3Z 12A/1Z12

THEORY:

Zener Diode: A zener diode is a silicon pn-junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of a zener diode is set by carefully controlling the doping level during manufacture. When a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically, and this is the key to zener diode operation. This volt-ampere characteristic is shown again in Figure- 1 with the normal operating region for zener diodes shown as a shaded area.

Zener Breakdown: Zener diodes are designed to operate in reverse breakdown. Two types of reverse breakdown in a zener diode are avalanche and zener. The avalanche effect, occurs in both rectifier and zener diodes at a sufficiently high reverse voltage. Zener breakdown occurs in a zener diode at low reverse voltages. A zener diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the zener breakdown voltage (V_Z), the field is intense enough to pull electrons from their valence bands and create current. Zener diodes with breakdown voltages of less than approximately 5 V operate predominately in zener breakdown. Those with breakdown voltages greater than approximately 5 V operate predominately in avalanche breakdown. Both types, however, are called zener diodes. Zeners are commercially available with breakdown voltages from less than 1 V to more than 250 V with specified tolerances from 1% to 20%.

Zener Regulation: Figure-2 shows the reverse portion of a zener diode's characteristic curve. Notice that as the reverse voltage (V_R) is increased, the reverse current (I_R) remains extremely small up to the "knee" of the curve. The reverse current is also called the zener current, I_Z. At this point, the breakdown effect begins; the internal zener resistance, also called zener impedance (Z_Z), begins to decrease as the reverse current increases rapidly.

From the bottom of the knee, the zener breakdown voltage (V_Z) remains essentially constant although it increases slightly as the zener current, I_Z, increases.

Zener Regulation is the ability to keep the reverse voltage across its terminals essentially constant is the key feature of the zener diode. A zener diode operating in breakdown acts as a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse-current values. A minimum value of reverse current, I_{ZK}, must be maintained in order to keep the diode in breakdown for voltage regulation. When the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also, there is a maximum current, I_{ZM}, above which the diode may be damaged due to excessive power dissipation. So, basically, the zener diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from I_{ZK} to I_{ZM}. A nominal zener voltage, V_Z, is usually specified on a datasheet at a value of reverse current called the zener test current.

To prevent high current through the Zener (for it may be damaged), a series resistor is included. After breakdown the voltage across the zener remains constant even if the input voltage varies or the load current changes.

PROCEDURE:

A. For Characteristic of Zener diode and measuring the Breakdown Voltage:

1. Connect the circuit as shown. Fix the load resistance to 2.2 K
2. Vary V_{in} and note the values of I_i, I_Z and V_Z/Vdc.
3. Tabulate the readings in table given below:
4. Draw V-I characteristics for the zener.
5. Find out the Breakdown Voltage (V_z) of the Zener diode

V_i (volts)	I_i (mA)	I_z (mA)	V_Z/V_{dc} (volts)

B. For Study Voltage regulation Characteristic of Zener diode:

1. Keep $V_{in} > V_z$ (fixed)
2. Vary load (By connecting different load resistances) and measure I_i , I_z and V_Z/V_{dc}.
3. Tabulate the readings in table given below.
4. Plot the variation in V_Z against R_L.

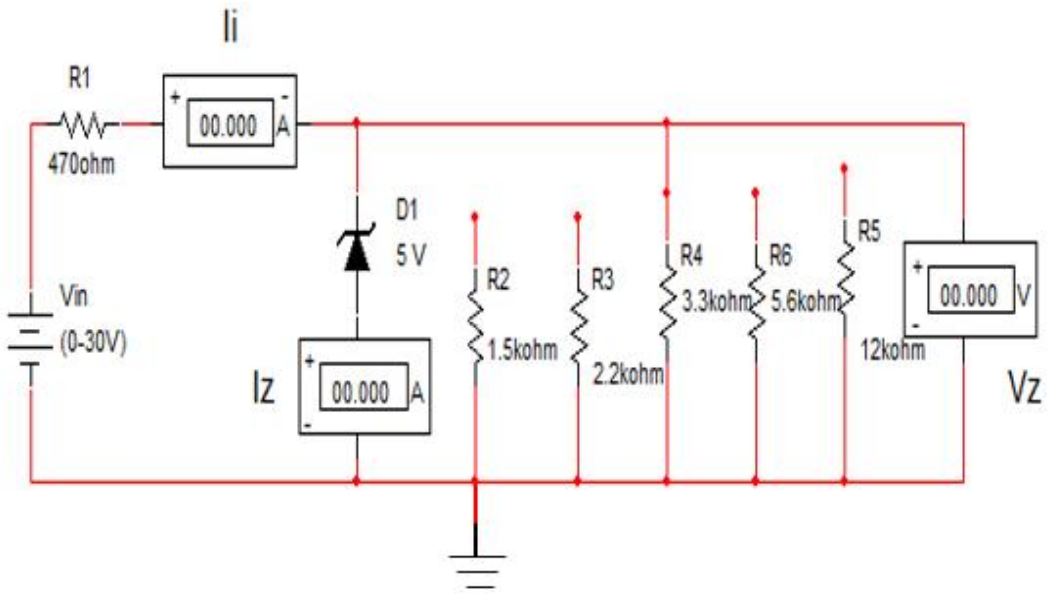
R_L (kΩ)	I_i (mA)	I_z (mA)	V_Z/V_{dc} (volts)
1.5			
2.2			
3.3			
5.6			
12			

RESULT & DISCUSSION:

PRECAUTIONS:

1. The polarities of diodes should be carefully identified.
2. While doing the experiment, do not exceed the ratings of the diode. This may lead to damage the diode.
3. Connect Voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
4. Do not switch-on the power supply unless you have checked the circuit connections as per the circuit diagram.
5. Readings should be taken carefully.
6. Power supply should be switched-off after completion of experiment.

EXPERIMENTAL SETUP:



(Circuit diagram to find Zener diode characteristics)

MODEL GRAPHS:

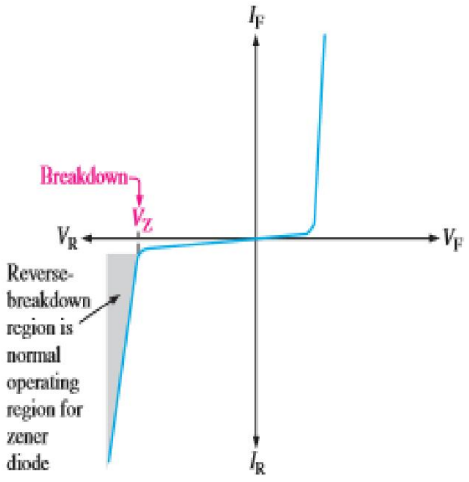


Fig-1
(Zener diode V-I Characteristic)

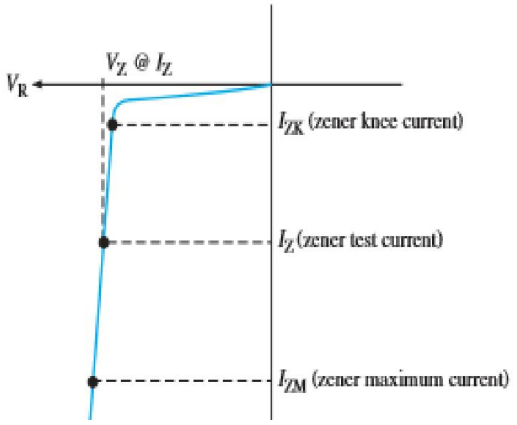


Fig-2
(Reverse characteristic of a Zener diode. V_Z is usually specified at a value of the Zener current known as the test current.)

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EXPERIMENT NO - 4

MEASUREMENT OF RECTIFICATION EFFICIENCY AND RIPPLE FACTOR OF HALF-WAVE AND FULL-WAVE RECTIFIER CIRCUITS WITH AND WITHOUT C-FILTER

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Measurement of rectification efficiency and ripple factor of Half-wave and Full-Wave rectifier circuits with and without C-Filter.

APPARATUS REQUIRED:

1. Power Supply
2. CRO.
3. Multimeter
4. Half Wave and Full Wave Rectifier Circuits
5. Circuit Board

CIRCUIT COMPONENTS:

1. Capacitor C=500μF
2. Resistor R_L=1KΩ

THEORY:

Because of their ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert ac voltage into dc voltage. Rectifiers are found in all dc power supplies that operate from an ac voltage source. A power supply is an essential part of each electronic system from the simplest to the most complex.

Half-Wave Rectifier: During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R_L. Hence the current produces an output voltage across the load resistor R_L, which has the same shape as the +ve half cycle of the input voltage.

During the negative half cycle of the input voltage, the diode is reverse biased and there is no current through the circuit i.e. the voltage across R_L is zero. The net result is only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified output voltage is the value measured on dc-voltmeter.

Full-Wave Rectifier: The circuit of a center-tapped full wave rectifier uses two diodes D1 & D2. During the positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2 is reverse biased. The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current flow.

The difference between full wave and half wave rectification is that, a full wave rectifier allows unidirectional current to the load during the entire 360 degrees of the input signal and half wave rectifier allows this only during one half cycle i.e. 180 degrees.

For practical circuits, transformer coupling is usually provided for two reasons:

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

A filter ideally eliminates the fluctuations in the output voltage of a half wave or full-wave rectifier and produces a constant-level dc voltage. Filtering is necessary because electronic circuits require a constant source of dc voltage and current to provide power and biasing for proper operation.

Ripple Factor

The output of a rectifier consists of a d.c. component and an a.c. component (also known as ripple). The a.c. component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of a.c. component in the output; the smaller this component, the more effective is the rectifier.

The ratio of r.m.s. value of a.c. component to the d.c. component in the rectifier output is known as ripple factor i.e.

Ripple factor (r) is defined as;

$$r = \frac{rms\ value\ of\ the\ a.c.component}{d.c.value\ of\ the\ rectifier\ wave} = \frac{I_{ac,rms}}{I_{dc}}$$

Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective a.c. component and hence more effective is the rectifier.

Rectification Efficiency

The ratio of d.c. power output to the applied input a.c. power is known as Rectification Efficiency.

Rectification Efficiency or Ratio of Rectification (η) is defined as;

$$\eta = \frac{d.c.\ power\ delivered\ to\ load}{a.c.\ input\ power\ from\ the\ Transformer} = \frac{P_{dc}}{P_{ac}}$$

PROCEDURE:

1. Connect a multimeter in series and a CRO in shunt across the load.
2. Connect the circuit as a Half wave rectifier without filter (K_1 and K_2 are open) and with C-filter (K1 is open and K2 is short). Tabulate readings of $I_{ac,rms}$ and I_{dc} without filter and with C-filter.
3. Calculate ripple factor (r),rectification efficiency (η) without filter and with C-filter. Compare these measured values with their respective theoretical values.
4. Observe waveforms on CRO.
5. Again connect the circuit as a Full wave rectifier without filter (K_1 is short and K_2 is open) and with C-filter (K_1 and K_2 are short). Tabulate readings of $I_{ac,rms}$ and I_{dc} without filter and with C-filter.
6. Calculate ripple factor (r),rectification efficiency (η) without filter and with C-filter. Compare these measured values with their respective theoretical values.
7. Observe waveforms on CRO.

OBSERVATIONS:

Type of Rectification	$I_{ac,rms}$	I_{dc}	I_{rms}	Ripple Factor (r)	Rectification Efficiency (η)
Half Wave Rectifier (without filter)					
Half Wave Rectifier (with C-filter)					
Full Wave Rectifier (without filter)					
Full Wave Rectifier (with C-filter)					

Note:

$$I_{rms} = \sqrt{(I_{ac,rms}^2 + I_{dc}^2)}$$

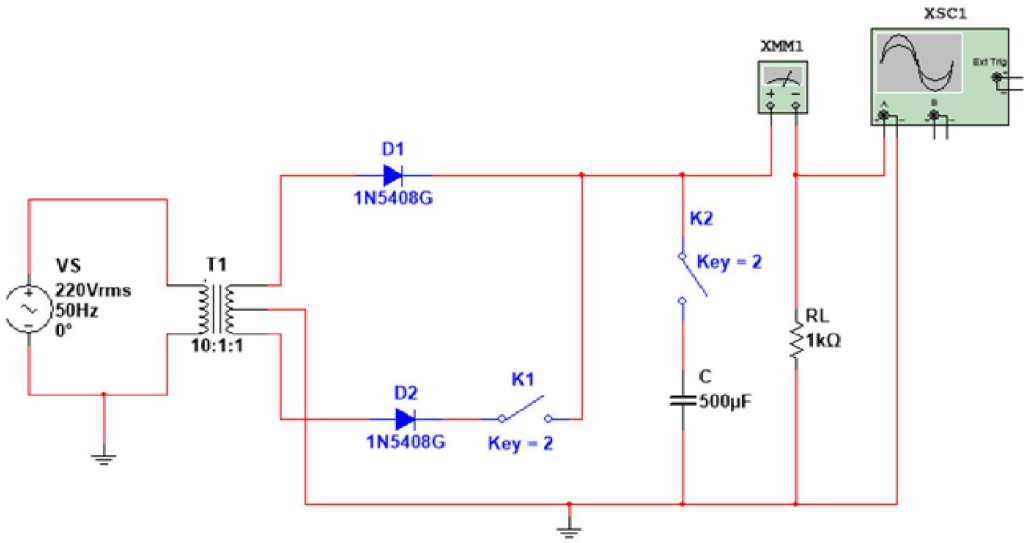
$$\eta = \frac{P_{dc}}{P_{ac}} = \left(\frac{I_{dc}}{I_{rms}}\right)^2 . \left(\frac{R_L}{R_f + R_L}\right) \approx \left(\frac{I_{dc}}{I_{rms}}\right)^2 ; \quad for\ R_f \ll R_L$$

RESULT & DISCUSSION:

PRECAUTIONS:

1. Do not use open ended wires for connecting to 220V power supply.
2. Before connecting the power supply plug in to socket, ensure power supply should be switched-off.
3. The primary and secondary sides of the transformer should be carefully identified.
4. The polarities of diodes should be carefully identified.
5. Ensure all connections should tight before switching-on the power supply.
6. Take the readings carefully.
7. Power supply should be switched-off after completion of experiment.

EXPERIMENTAL SETUP:



(Circuit diagram of Half-Wave and Full-Wave Diode Rectifier)

APPENDIX

RIPPLE FACTOR

RIPPLE FACTOR (WITHOUT FILTER)

Half-Wave Rectifier without Filter:

Ripple factor $r = \frac{I_{ac,rms}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{\left(I_m/2\right)^2}{\left(I_m/\pi\right)^2}} - 1 = 1.21$

Full-Wave Rectifier without Filter:

Ripple factor $r = \frac{I_{ac,rms}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\frac{\left(I_m/\sqrt{2}\right)^2}{\left(2I_m/\pi\right)^2}} - 1$

$= 0.482$

RIPPLE FACTOR (WITH SHUNT CAPACITOR FILTER)

As the name suggests, a capacitor is used as the filter and this high value capacitor is shunted or placed across the load impedance. This capacitor, when placed across a rectifier gets charged and stores the charged energy during the conduction period. When the rectifier is not conducting, this energy charged by the capacitor is delivered back to the load. Through this energy storage and delivery process, the time duration during which the current flows through the load resistor gets increased and the ripples are decreased by a great amount. Thus for the ripple component with a frequency of 'f' megahertz, the capacitor 'C' will offer a very low impedance. The value of this impedance can be written as:

Shunt Capacitor Impedance = $\frac{1}{2fC}$

Thus the dc components of the input signal along with the few residual ripple components, is only allowed to go through the load resistance R_L. The high amount of ripple components of current gets bypassed through the capacitor C.

Half-Wave Rectifier with Shunt Capacitor Filter:

The circuit diagram Fig.-1, shows a half-wave rectifier with a capacitor filter. The filter is applied across the load R_L. The output of the R_L is V_L, the current through it is I_L. The current through the capacitor is Ic.

During the positive half cycle of the input ac voltage, the diode D will be forward biased and thus starts conducting. During this period, the capacitor 'C' starts charging to the

maximum value of the supply voltage Vsm. When the capacitor is fully charged, it holds the charge until the input ac supply to the rectifier reaches the negative half cycle. As soon as the negative half supply is reached, the diode gets reverse biased and thus stops conducting. During the non-conducting period, the capacitor 'C' discharges all the stored charges through the output load resistance R_L. As the voltage across R_L and the voltage across the capacitor 'C' are the same (V_L = Vc), they decrease exponentially with a time constant ($C*R_L$) along the curve of the non-conducting period. This is shown in the graph below, Fig.-2.

The value of the discharge time constant ($C*R_L$) being very large, the capacitor 'C' will not have enough time to discharge properly. As soon as the capacitor starts discharging, the time becomes over. Thus the value of R_L at the discharge time will also be high and have just a little less value that the output of R_L. This is when the positive half cycle repeats again and the diode starts conducting. The condition to be considered at this stage is that the rectified voltage takes value more than the capacitor voltage. When the condition occurs the capacitor starts charging to a value of Vsm. The condition again changes when the negative half cycle comes into pace, and the whole cycle is again repeated to form the output waveform as shown above. The output shows a nearly constant dc voltage at the load and that the output voltage is increased considerably.

Thus, in short:
If the value of load resistance is large, the discharge time constant will be of a high value, and thus the capacitors' time to discharge will get over soon. This lowers the amount of ripples in the output and increases the output voltage. If the load resistance is small, the discharge time constant will be less, and the ripples will be more with decrease in output voltage.

- The value of the capacitor used plays an important role in determining the output ripples and the average dc level. If the capacitor value is high, the amount of charge it can store will be high and the amount it discharges will be less. Thus the ripples will be less and the average dc level will be high. But, there is a limit on how much capacitance can be increased. If the capacitor value is increased to a very high value, the amount of current required to charge the capacitor to a given voltage will be high. This value of current depends on the manufacturer of the diode and will be surely limited to a certain value. Thus, there is a limit in increasing the capacitor value in a half-wave rectifier shunt capacitor filter circuit.
- Poor voltage regulation.

Ripple Factor with C-Filter

The rms value depends on the peak value of charging and discharging magnitude, $V_{r,pp}$

$$V_{r,rms} = \frac{V_{r,pp}}{2\sqrt{3}}$$

$$V_{r,pp} = \frac{I_{dc}}{f.C}$$

$$Ripple\ factor\ (r) = \frac{V_{r,rms}}{V_{dc}} = \frac{V_{r,pp}/2\sqrt{3}}{V_{dc}} = \frac{I_{dc}}{2\sqrt{3}f.C}.\frac{1}{I_{dc}.R_L} = \frac{1}{2\sqrt{3}f.C.R_L}$$

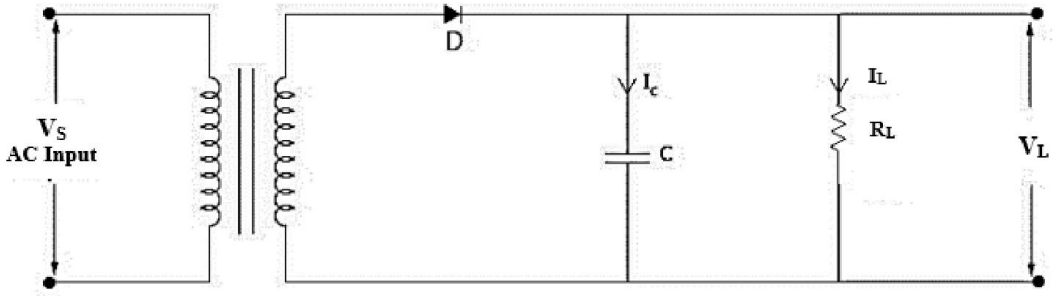


Fig.-1 (Half-wave Rectifier with C-Filter)

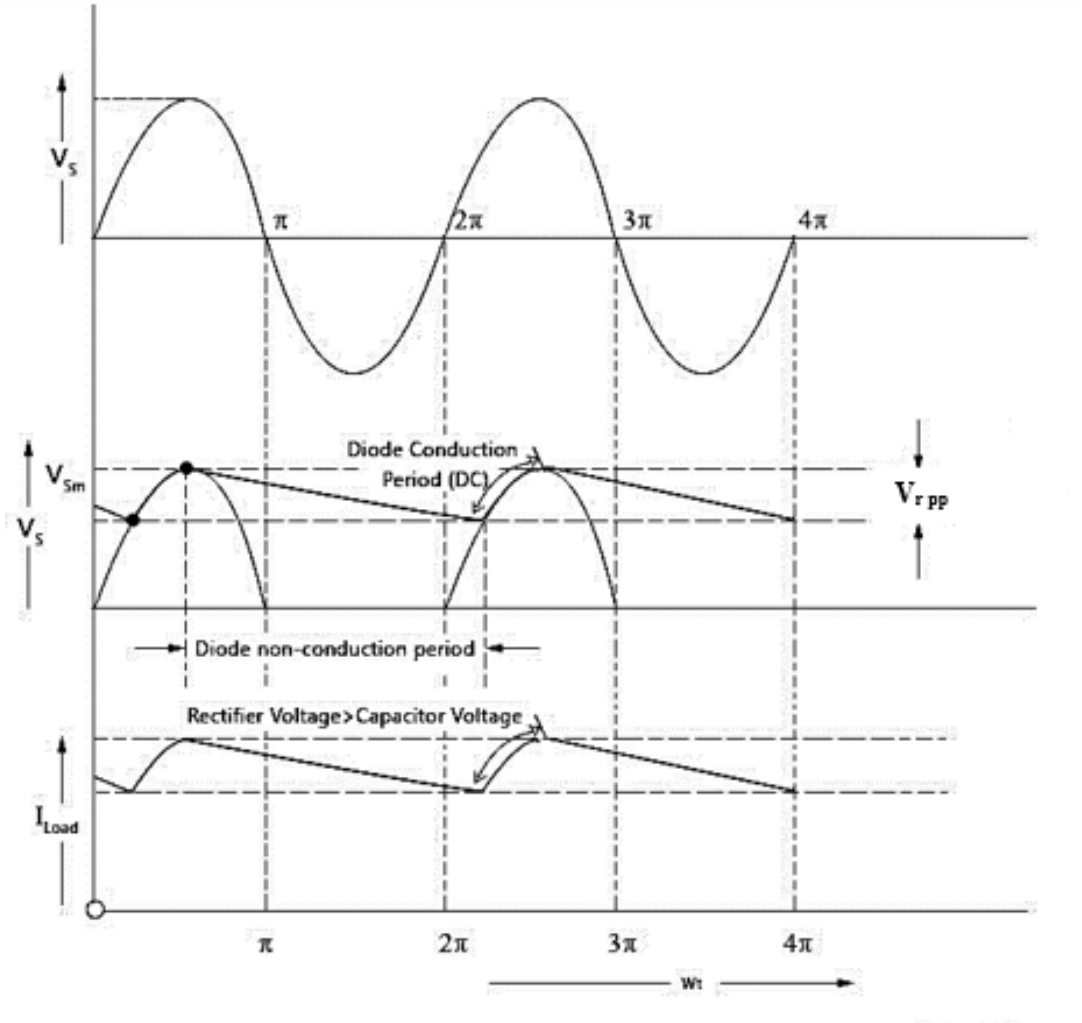


Fig.-2 (Half-wave Rectifier with Capacitor Filter – Waveform)

Full-Wave Rectifier with Shunt Capacitor Filter:

The circuit diagram Fig.-3, shows a full-wave rectifier with a capacitor filter. The filter capacitor C is placed across the resistance load R_L. The whole working is pretty much similar to that of a half-wave rectifier with shunt capacitor explained above. The only difference is that two pulses of current will charge the capacitor during alternate positive (D1) and negative (D2) half cycles. Similarly capacitor C discharges twice through R_L during one full cycle. This is shown in the waveform below, Fig.-4.

The load current reduces by a smaller amount before the next pulse is received as there are 2 current pulses per cycle. This causes a good reduction in ripples and a further increase in the average dc load current.

Ripple Factor with C-Filter

The rms value depends on the peak value of charging and discharging magnitude, $V_{r,pp}$

$$V_{r,rms} = \frac{V_{r,pp}}{2\sqrt{3}}$$

$$V_{r,pp} = \frac{I_{dc}}{2f.C}$$

$$Ripple\ factor\ (r) = \frac{V_{r,rms}}{V_{dc}} = \frac{V_{r,pp}/2\sqrt{3}}{V_{dc}} = \frac{I_{dc}}{4\sqrt{3}f.C}.\frac{1}{I_{dc}.R_L} = \frac{1}{4\sqrt{3}f.C.R_L}$$

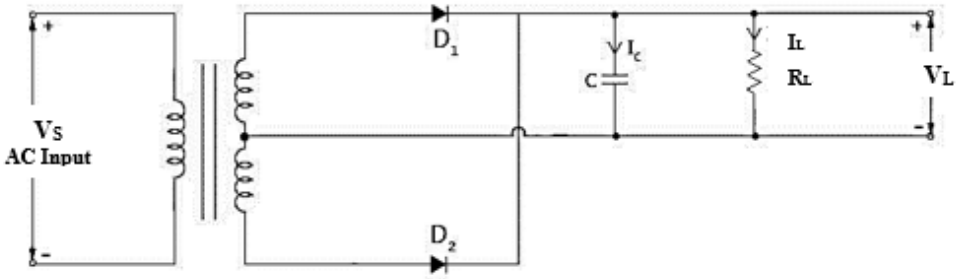


Fig.-3 (Full-wave Rectifier with C-Filter)

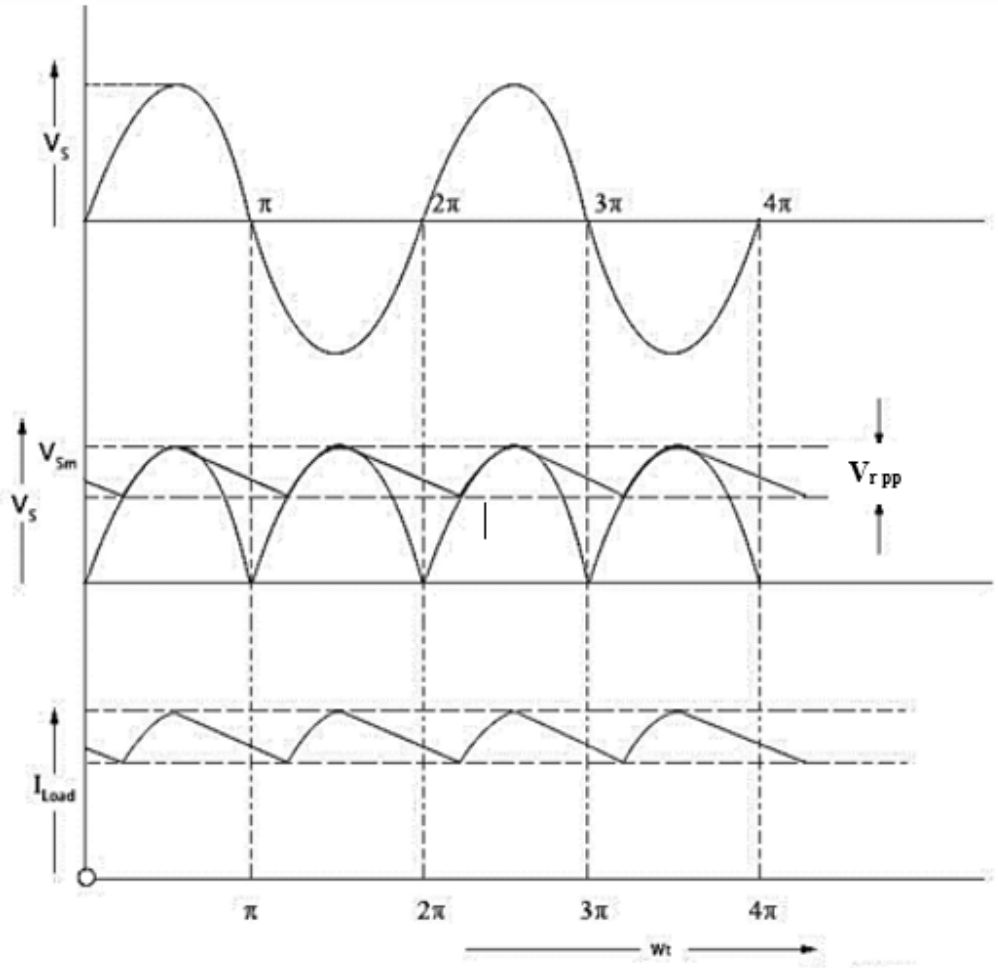


Fig.-4 (Full-wave Rectifier with C-Filter – Waveform)

RECTIFICATION EFFICIENCY

Rectification Efficiency of HW-Rectifier:

Rectification efficiency is defined as the ratio between the dc-output power to the ac-input power.

i.e. $$\eta = \frac{\text{dc power delivered to the load}}{\text{ac input power from the transformer}} = \frac{P_{dc}}{P_{ac}}$$

The dc power delivered to the load,

$$P_{dc} = I_{dc}^2 . R_L = \left(\frac{I_m}{\pi}\right)^2 . R_L$$

The ac power input to the transformer,

$$P_{ac} = I_{rms}^2 . R_f + I_{rms}^2 . R_L = \left({I_m^2}/{4}\right) . \left(R_f + R_L\right)$$

So, Rectification Efficiency,

$$\eta = \frac{P_{dc}}{P_{ac}} = \left(\frac{4}{\pi^2}\right) . \left(\frac{R_L}{R_f + R_L}\right) = \frac{0.406}{1 + {R_f}/{R_L}}$$

The maximum efficiency that can be obtained by the half wave rectifier is **40.6 %.** This is obtained if R_f is neglected.

Rectification Efficiency of FW-Rectifier:

The dc power delivered to the load,

$$P_{dc} = I_{dc}^2 . R_L = \left(\frac{2I_m}{\pi}\right)^2 . R_L$$

The ac power input to the transformer,

$$P_{ac} = I_{rms}^2 . R_f + I_{rms}^2 . R_L = \left({I_m^2}/{2}\right) . \left(R_f + R_L\right)$$

So, Rectification Efficiency,

$$\eta = \frac{P_{dc}}{P_{ac}} = \left(\frac{8}{\pi^2}\right) . \left(\frac{R_L}{R_f + R_L}\right) = \frac{0.8105}{1 + {R_f}/{R_L}}$$

The maximum efficiency that can be obtained by the full wave rectifier is **81.05 %.** This is obtained if R_f is neglected.

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EXPERIMENT NO - 5

TO DETERMINE THE FREQUENCY RESPONSE OF CE TRANSISTOR AMPLIFIER AND FINDING ITS GAIN-BANDWIDTH PRODUCT

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: To determine the frequency response of CE transistor amplifier and finding its gain-bandwidth product.

APPARATUS REQUIRED:

1. Power Supply
2. Function Generator
3. AC Milli Voltmeter
4. Common Emitter Transistor Amplifier Circuit

CIRCUIT COMPONENTS:

1. Capacitors, C1=50μF, C2=50μF, C3=250μF
2. Resistors, R1=1KΩ, R2=8.2KΩ, R3=1.5KΩ, R4=1KΩ, R5=470Ω, R6=1KΩ

THEORY:

The Amplifier is an electronic circuit that is used to increase the strength of a weak input signal in terms of voltage, current, or power. The process of increasing the strength of a weak signal is known as Amplification. One most important constraint during the amplification is that only the magnitude of the signal should increase and there should be no changes in original signal shape. The transistor (BJT, FET) is a major component in an amplifier system. When a transistor is used as an amplifier, the first step is to choose an appropriate configuration, in which device is to be used. Then, the transistor should be biased to get the desired Q-point. The signal is applied to the amplifier input and output gain is achieved. In this article, we will discuss common emitter amplifier analysis.

Common Emitter Amplifier Configuration: In Common Emitter Amplifier Configuration, the Emitter of a BJT is common to both the input and output signal as shown below. The arrangement is the same for a NPN transistor, but bias will be opposite w.r.t PNP transistor.

Operation of Common Emitter Amplifier: When a signal is applied across the emitter-base junction, the forward bias across this junction increases during the upper half cycle. This leads to increase the flow of electrons from the emitter to a collector through the base, hence increases the collector current. The increasing collector current makes more voltage drops across the collector load resistor R_C=R3. The negative half cycle decreases the

forward bias voltage across the emitter-base junction. The decreasing collector-base voltage decreases the collector current in the whole collector resistor R3. Thus, the amplified load resistor appears across the collector resistor. It is seen that there is a 180-degree phase shift between the input and output waveforms.

Common Emitter Amplifier Circuit Elements and Their Functions:

Biasing Circuit/ Voltage Divider: The resistances R2, R4 and R5 used to form the voltage biasing and stabilisation circuit. The biasing circuit needs to establish a proper operating Q-point otherwise, a part of the negative half cycle of the signal may be cut-off in the output.

Input Capacitor (C1):

The capacitor C1 is used to couple the signal to the base terminal of the BJT. If it is not there, the signal source resistance, R1 will come across R4 and hence, it will change the bias. C1 allows only the AC signal to flow but isolates the signal source from R4.

Emitter Bypass Capacitor (C3):

An Emitter bypass capacitor C3 is used parallel with R5 to provide a low reactance path to the amplified AC signal. If it is not used, then the amplified AC signal following through R5 will cause a voltage drop across it, thereby dropping the output voltage.

Coupling Capacitor (C2):

The coupling capacitor C2 couples one stage of amplification to the next stage. This technique used to isolate the DC bias settings of the two coupled circuits.

Base current : $i_B = I_B + i_b$

where,

I_B = DC base current when no signal is applied.

I_b = AC base when AC signal is applied and i_B = total base current.

Collector current : $i_C = I_C + ic$

where,

i_C = total collector current.

I_C = zero signal collector current.

ic = AC collector current when AC signal is applied.

Emitter Current : $i_E = I_E + ie$

where,

I_E = Zero signal emitter current.

ie = AC emitter current when AC signal is applied.

i_E = total emitter current.

CE Amplifier Frequency Response: The voltage gain of a CE amplifier varies with signal frequency. It is because reactance of capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve drawn between voltage gain and the signal frequency of an amplifier is known as frequency response. Below model graph shows the frequency response of a typical CE amplifier.

From the model-graph, we observe that the voltage gain drops off at low (< FL) and high (> FH) frequencies, whereas it is constant over the mid-frequency range (FL to FH).

At low frequencies (< FL): The reactance of coupling capacitor C2 is relatively high and hence very small part of the signal will pass from amplifier stage to the load. Moreover, C3 cannot shunt the R5 effectively because of its large reactance at low frequencies. These two factors cause a drops off of voltage gain at low frequencies.

At high frequencies (> FH): The reactance of coupling capacitor C2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain. Moreover, at high frequencies, the capacitive reactance of base-emitters junction is low which increases the base current. This frequency reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

At mid frequencies (FL to FH): The voltage gain of the amplifier is constant. The effect of the coupling capacitor C2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of C2 decreases, which tend to increase the gain. However, at the same time, lower reactance means higher almost cancel each other, resulting in a uniform fair at mid-frequency.

PROCEDURE:

1. Connect the power supply to the circuits as shown. Set the voltage to –12 Volts with respect to common terminal.
2. Connect a function generator to the input terminal and set it to 25 mV, 10 Hz.
3. Connect an ac millivoltmeter to the output terminal.
4. Read the output and note down.
5. Keeping V_{in} fixed at 25 mV, go on increasing the frequency at regular intervals and measuring the output voltage.
6. Tabulate the readings.
5. Plot Gain against frequency on semi-logarithmic graph sheet.
6. Find 3dB point frequencies and Bandwidth.
7. Observe the input and output waveforms for one certain frequency in mid-band range.

Note: Try to take the reading until gain will drop from its constant gain up to the value, which is approximately equal to the gain value for first reading.

OBSERVATIONS:

Input Voltage (fixed) = 25 mV.

Frequency (Hz)	Output Voltage V_{out} (Volt)	Voltage Gain (V_{out}/ V_{in})	Gain [20 $\log_{10}$ (V_{out}/V_{in})] (dB)
10			
20			

100			
200			

1K			
2K			
3K			

10K			
20K			

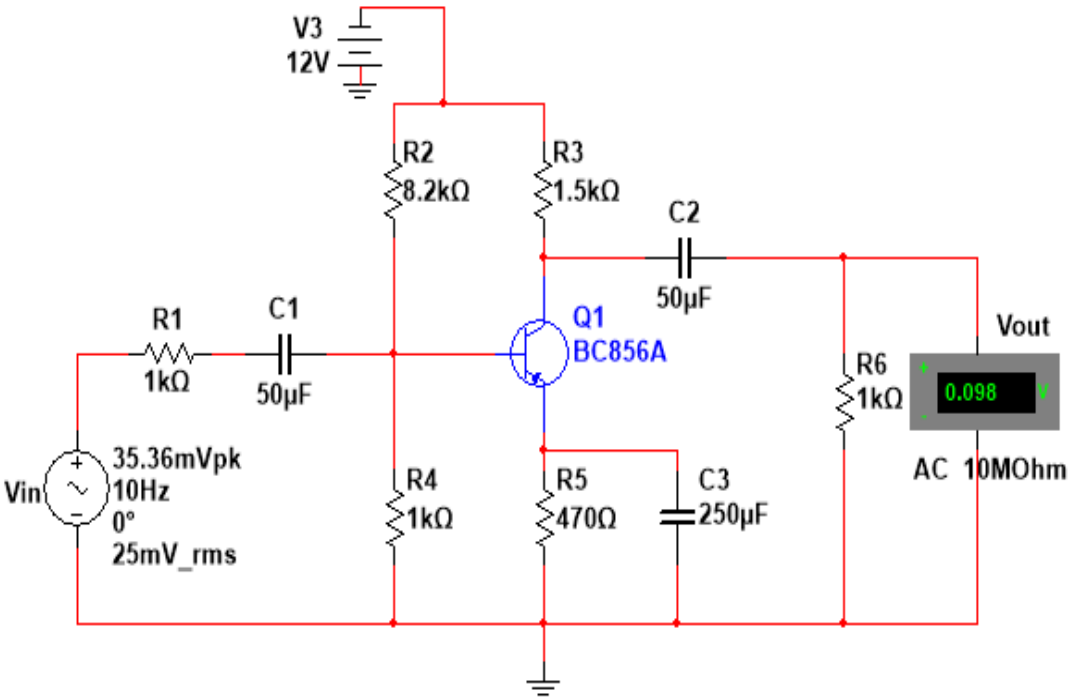
100K			
200K			

RESULT & DISCUSSION:

PRECAUTIONS:

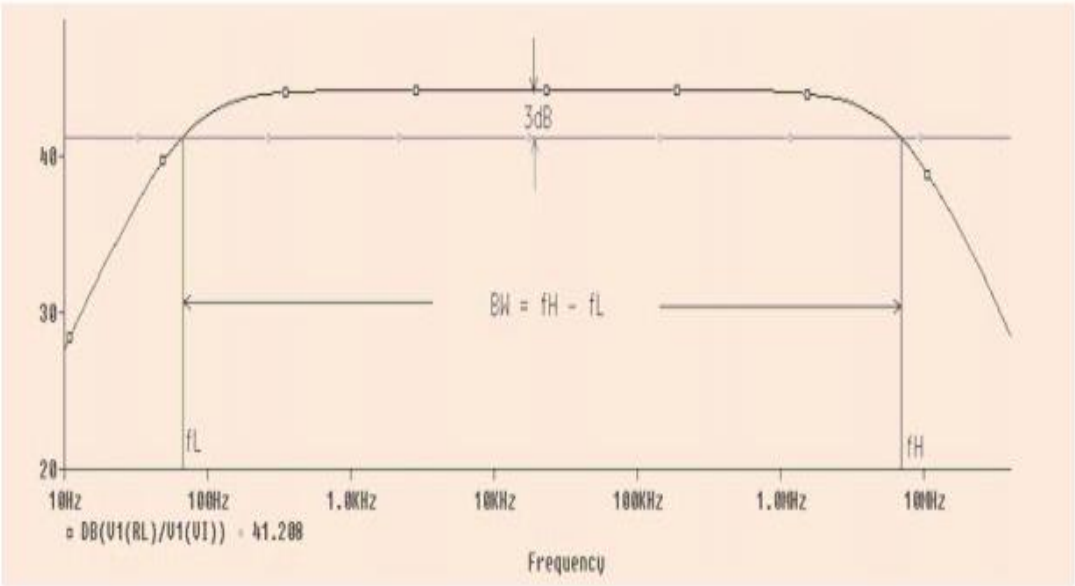
1. Do not use open ended wires for connecting to 220V power supply.
2. Before connecting the power supply plug in to socket, ensure power supply should be switched-off.
3. Ensure all connections should tight before switching-on the power supply.
4. Readings should be taken carefully.
5. Power supply should be switched-off after completion of experiment.

EXPERIMENTAL SETUP:



(Circuit diagram for Common Emitter Amplifier)

MODEL GRAPH:



Frequency Response of Common Emitter Amplifier

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LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

EXPERIMENT NO-6

TO DETERMINE THE OUTPUT AND TRANSFER CHARACTERISTICS OF JFET AND MEASUREMENT OF ITS VOLTAGE GAIN

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: To determine the output and transfer characteristics of JFET and measurement of its voltage gain.

APPARATUS REQUIRED:

1. Bread Board
2. Power Supply
4. Milliammeter
5. Electronic Multimeter

CIRCUIT COMPONENTS:

1. JFET-BFW 10/11
2. Resistors, R=1KΩ, R_d=1KΩ

THEORY:

A field effect transistor is a three-terminal unipolar device. Its input impedance is very high. A field effect transistor can be either a JFET or MOSFET. A JFET, MOSFET both can be either have N-channel or P-channel. An N-channel JFET has an N-type Semiconductor bar, the two ends of which make the drain and source terminals. On the other two sides of this N-type Semiconductor bar, two P type regions are made. These P-regions form gates. Usually, these two Gates are connected together to form a single gate. The gate is given a negative bias with respect to the source. The drain is given positive potential with respect to the source. In case of a P-channel JFET, the terminals of all the batteries are reversed.

JFET is a voltage controlled current device so its characteristics are the curves which represent relationship between different dc currents and voltages. These are helpful in studying different region of operation of a Field effect transistor when connected in a circuit. The two important characteristics of a Field Effect Transistor are:

1. Output /Drain characteristic.
2. Transfer characteristic.

Output / Drain Characteristics: It is the curve plotted between output drain current I_D verses output drain to source voltage V_{DS} for constant values of input Gate to source voltage V_{GS} as shown in Fig 1.

Ohmic region OA: This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

Curve AB: In this region, I_D increases at inverse square law rate up to point B which is called Pinch-off point. This progressive fall in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate up to point B where the two regions are closest without touching each other. The drain to source voltage V_{DS} corresponding to point B is called pinch-off voltage V_{PO}.

Pinch-off region BC: It is also known as saturation region or 'amplifier' region. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. Drain current in this region is given by Shockley's equation;

$$I_D = I_{DSS} [1 - (V_{GS} / V_{PO})^2] = I_{DSS} [- (V_{GS} / V_{GS\ (off)})^2]$$

It is the normal operating region of the JFET when used as an amplifier.

Breakdown region: If V_{DS} is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an extensive value. This happens because the reversed biased gate channel PN junction undergoes avalanche breakdown when small change in V_{DS} produce very large change in I_D.

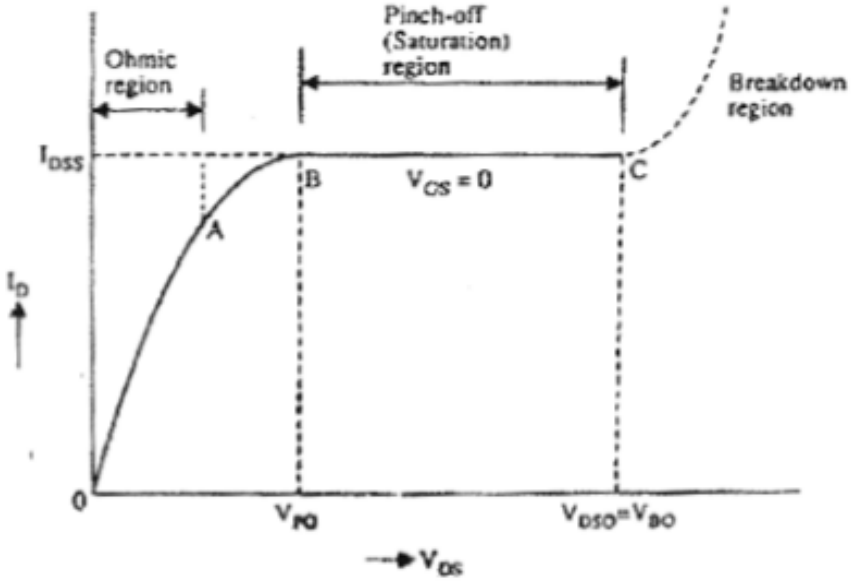


Fig-1

JFET characteristics with External Bias: Fig 2 shows a family of I_D verses V_{DS} curves for different values of V_{GS}. It is seen that as the negative gate bias voltage is increased: Pinch-off voltage V_P is reached at a lower value of V_{DS} than $V_{GS} = 0$. Value of V_{DS} for breakdown is decreased.

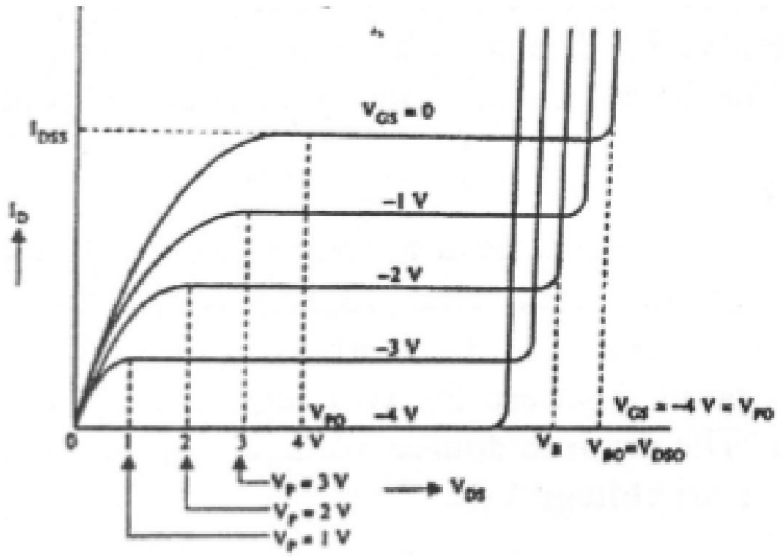


Fig-2

Transfer Characteristic: It is the curve plotted between output drain current versus input Gate to source voltage for constant values of output drain to source voltage as shown in Fig 3.

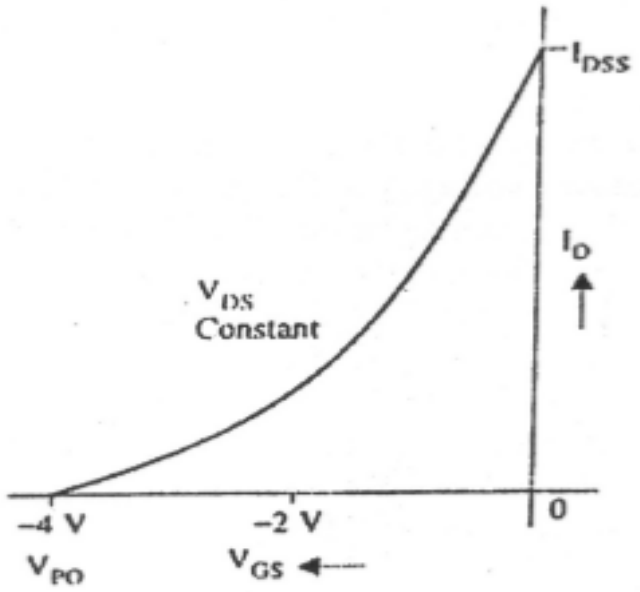


Fig-3

It is similar to the transconductance characteristics of a vacuum tube or a transistor. It is shows that when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $I_D = 0$, $V_{GS} = V_{PO}$. The transfer characteristic approximately follows the equation

$$I_D = I_{DSS} [1 - (V_{GS} / V_{PO})^2] = I_{DSS} [1 - (V_{GS} / V_{GS(off)})^2]$$

The above equation can be written as $V_{GS} = V_{GS(off)} [1 - (I_D / I_{DSS})^{1/2}]$. These characteristics can also be obtained from the drain/output characteristics by reading off V_{GS} and I_{DSS} values for different values of V_{DS}. The various parameters of a JFET can be obtained from its two characteristics.

The main parameters of a JFET when connected in common source mode are:

1. **AC Drain Resistance, r_d :** It is the ac resistance between drain and source terminals when JFET is operating in the pinch-off region. It is given by;

$$r_d = \frac{Change\ in\ V_{DS}}{Change\ in\ I_D} \quad ; \text{ At } V_{GS} \text{ constant}$$

   An alternative name is dynamic drain resistance. It is given by the slope of the drain characteristics in the pinch off region. It is sometimes written as rds emphasizing the fact that it is the resistance from drain to source. Since rd is usually the output resistance of a JFET, it may also be expressed as an output admittance Yds. Obviously, Yds = 1/rd. It has a very high value.

2. Transconductance, gm: It is simply the slope of transfer characteristics;

$$g_m = \frac{Change\ in\ I_D}{Change\ in\ V_{GS}} \quad ; \text{ At } V_{DS} \text{ constant}$$

Its unit is siemens (S) /mho. It is also called forward transconductance (g_{fs}) or forward transadmittance Y_{fs}. The transconductance measured at I_{DSS} is written as g_{mo}. Mathematically;

$$g_m = g_{mo} [1 - (V_{GS} / V_P)]$$

FORMULAE USED:

1. Drain Resistance $r_d = \Delta V_{DS}/\Delta Id \,|V_{GS}$=constant
2. Tran conductance $g_m = \Delta I_D/\Delta V_{GS} \,|V_{DS}$=constant
3. Amplification/Intrinsic factor of JFET
   $\mu = r_d * g_m = \Delta V_{DS}/\Delta V_{GS} \,|I_D$=constant

PROCEDURE:

(a) To plot the Drain characteristics

1. Assemble the circuit as shown in fig.
2. First, fix V_{GS} at some value say 0 V. Increase the drain voltage V_{DS} slowly from 0V to 10V, in steps of 0.5V. Note drain current I_D for each step.
3. Now, change V_{GS} to another value (say V_{GS} = -1V) and repeat the above steps for V_{GS} = -1V.
4. Plot the output characteristics (graph between I_D and V_{DS} for fixed value of $V_{GS)}$.
5. Find the drain resistance $r_d = \Delta V_{DS} / \Delta I_D$ with V_{GS} constant.

(b) To plot the Transfer characteristics

1. Adjust V_{DS} to a value say 5V and keep it constant throughout the observations.
2. Vary V_{GS} slowly from 0V to -5V, in steps of 0.5V and note I_D for each value.
3. Plot the Transfer characteristics (graph between I_D and V_{GS} for fixed value of $V_{DD)}$.
4. Find the Trans conductance. $g_m = \Delta I_D / \Delta V_{GS}$ with V_{DS} constant.

(c) Calculate Amplification/Intrinsic factor of JFET

$$\mu = r_d * g_m = \Delta V_{DS}/\Delta V_{GS} \,|I_D=\text{constant}$$

OBSERVATIONS:

OUTPUT CHARACTERISTICS:

SL.NO	V_{DS} (0V to 10V) In Steps of 0.5V	V_{GS} = 0V	V_{GS} = -1V
		I_D(mA)	I_D(mA)
1.	0 V		
2.	0.5V		
3.	1V		
---	---		
---	---		
20.	9.5V		
21.	10V		

TRANSFER CHARACTERISTICS:

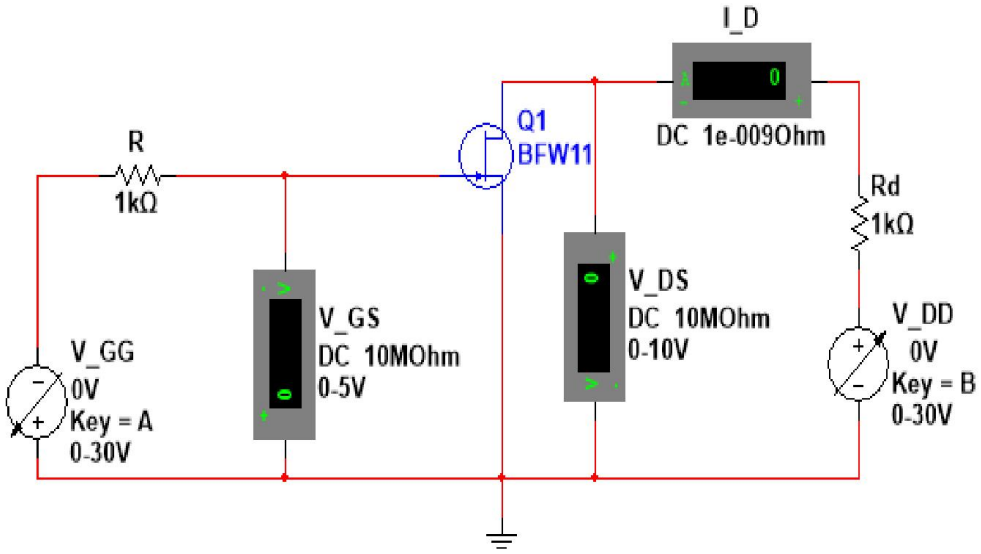
SL.NO	V_{GS} (0V to -5V) In Steps of 0.5V	V_{DS} kept Constant at 5V (V_{DS} = 5V)
		I_D(mA)
1.	0 V	
2.	-0.5V	
3.	-1V	
---	---	
---	---	
10.	-4.5V	
11.	-5V	

RESULT & DISCUSSION:

PRECAUTIONS:

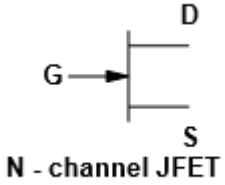
1. The three terminals of the JFET must be carefully identified
2. Practically JFET contains four terminals, which are called Source, Drain, Gate, Substrate.
3. Source and Case should be short circuited.
4. Voltages exceeding the ratings of the JFET should not be applied.
5. Readings should be taken carefully.

EXPERIMENTAL SETUP:

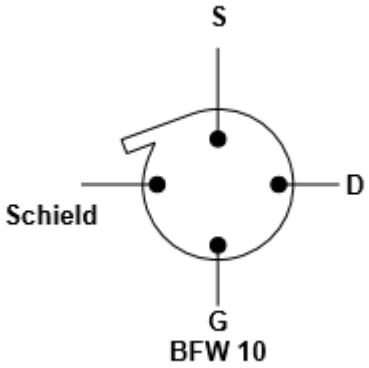


(Circuit diagram for measurement of Output and Transfer Characteristics of JFET)

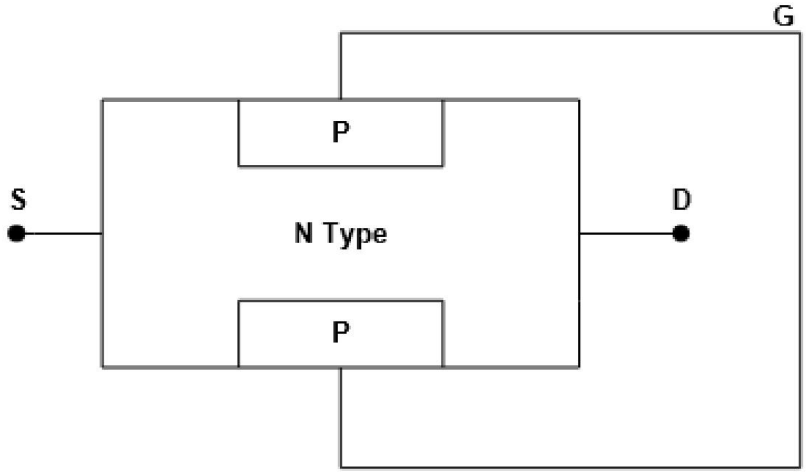
KEY REFERENCES:



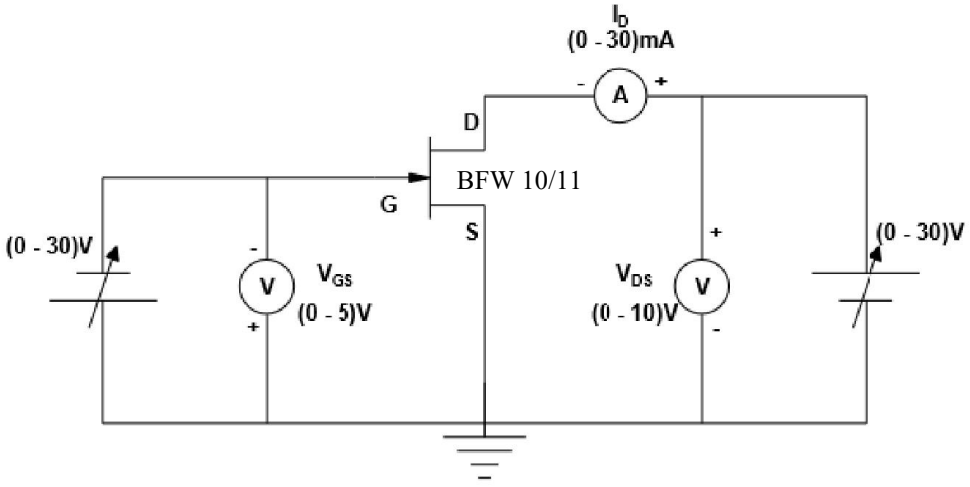
(Symbol of N-Channel JFET)



(Pin Diagram of N-Channel JFET)



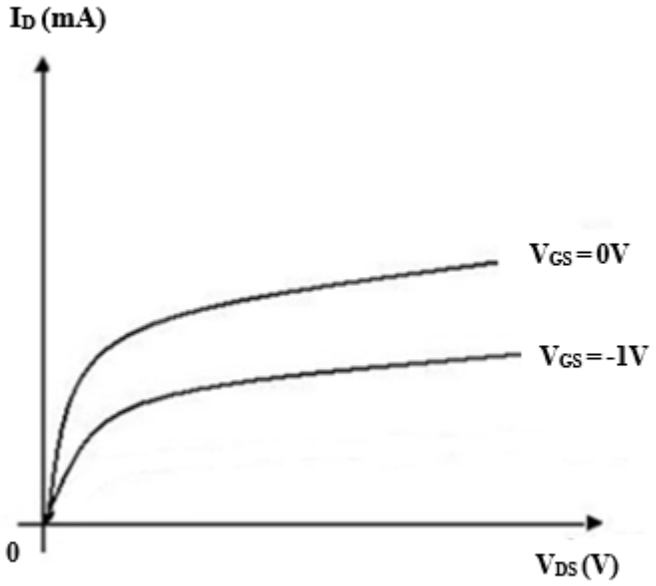
(Construction of N-Channel JFET)



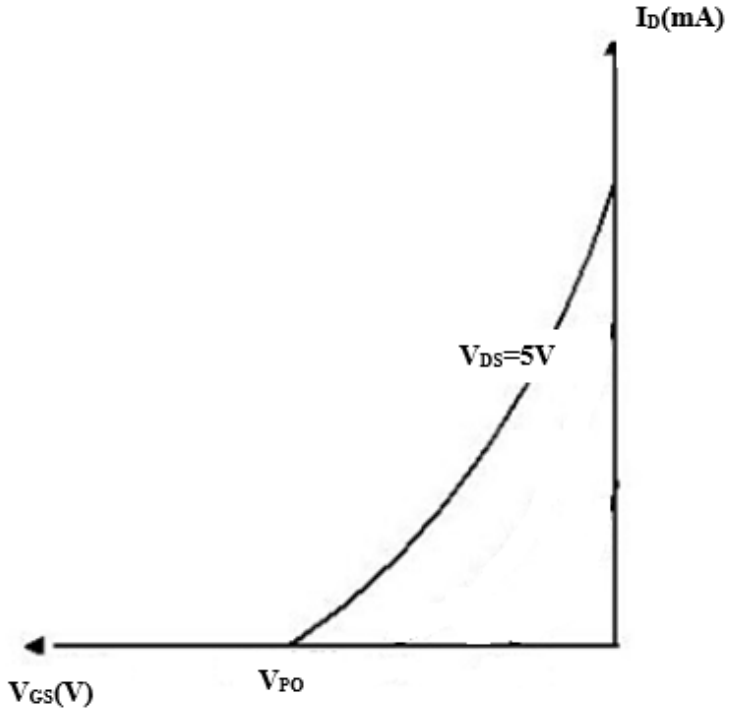
(Circuit Connection of N-Channel JFET)

MODEL GRAPHS:

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



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EC102: ELECTRONICS & COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

EXPERIMENT NO - 7

DESIGN OF RC PHASE SHIFT OSCILLATOR USING IC 741 OP-AMP AND FINDING ITS FREQUENCY OF OSCILLATION

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Design of RC Phase Shift Oscillator using IC 741 OP-AMP and finding its frequency of oscillation.

APPARATUS REQUIRED:

1. Dual DC Power Supply
2. CRO
3. Bread Board

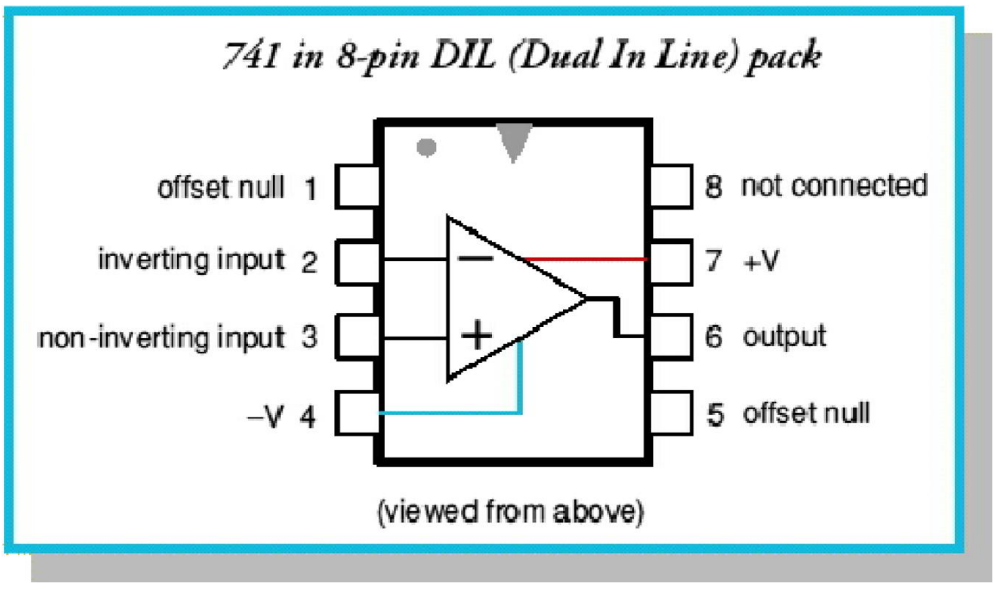
CIRCUIT COMPONENTS:

1. IC 741
2. Resistor 8.2KΩ, 10KΩ, 33KΩ, 470KΩ
3. Capacitor 0.1μF

THEORY:

ABOUT OP-AMP IC 741

The 741 is the godfather of all operational amplifiers (amplifiers on a chip). Although most up-to-date designs beat it for speed, low noise, etc., it still works well as a general purpose device. One of its advantages is that it is *compensated* (its frequency response is tailored) to ensure that under most circumstances it won't produce unwanted spurious oscillations. This means it is easy to use, but the down-side of this is the poor speed/gain performance compared to more modern op-amps.



The 741 is usually supplied in an 8-pin 'DIL' (Dual In Line) or 'DIP' (Dual Inline Package, or sometimes Dual Inline Plastic) package with a pinout shown above. This has proved so popular that many other competing op-amps have adopted the same package/pinout. Hence for many applications the various op-amps are 'drop in' replacements or upgrades for one another. These days there is a large family of 741 type devices, made by various manufacturers. Sometimes one manufacturer will make different versions, which work better than others in some respect. Each has a slightly different part number, but it generally has "741" in it somewhere!

The values given below are 'typical' for an ordinary 741, better versions (more expensive) may give better results...

```
Typical values of Basic Parameters:
Rail voltages : +/- 15V dc (+/- 5V min, +/- 18V max)
Input impedance: Around 2MegOhms
Low Frequency voltage gain: approx 200,000
Input bias current: 80nA
Slew rate: 0.5V per microsecond
Maximum output current: 20mA
Recommended output load: not less than 2kilOhms
```

Note that, due to the frequency compensation, the 741's voltage gain falls rapidly with increasing signal frequency. Typically down to 1000 at 1kHz, 100 at 10kHz, and unity at about 1MHz. To make this easy to remember we can say that the 741 has a *gain bandwidth product* of around one million (i.e. 1 MHz as the units of frequency are Hz).

RC PHASE SHIFT OSCILLATOR:

The RC phase shift oscillator consists of an op-amp as amplifier and 3 RC cascade networks as the feedback circuit. The op-amp is used in the inverting mode, so output signal will be 180˚ out of phase. The feedback RC network provides the exactly 180˚ phase shift. So the total phase shift is 0˚. The gain of the amplifier is also kept large to produce oscillation.

The frequency of oscillation is given by;

$$f = 0.065/\mathrm{RC}$$

PROCEDURE:

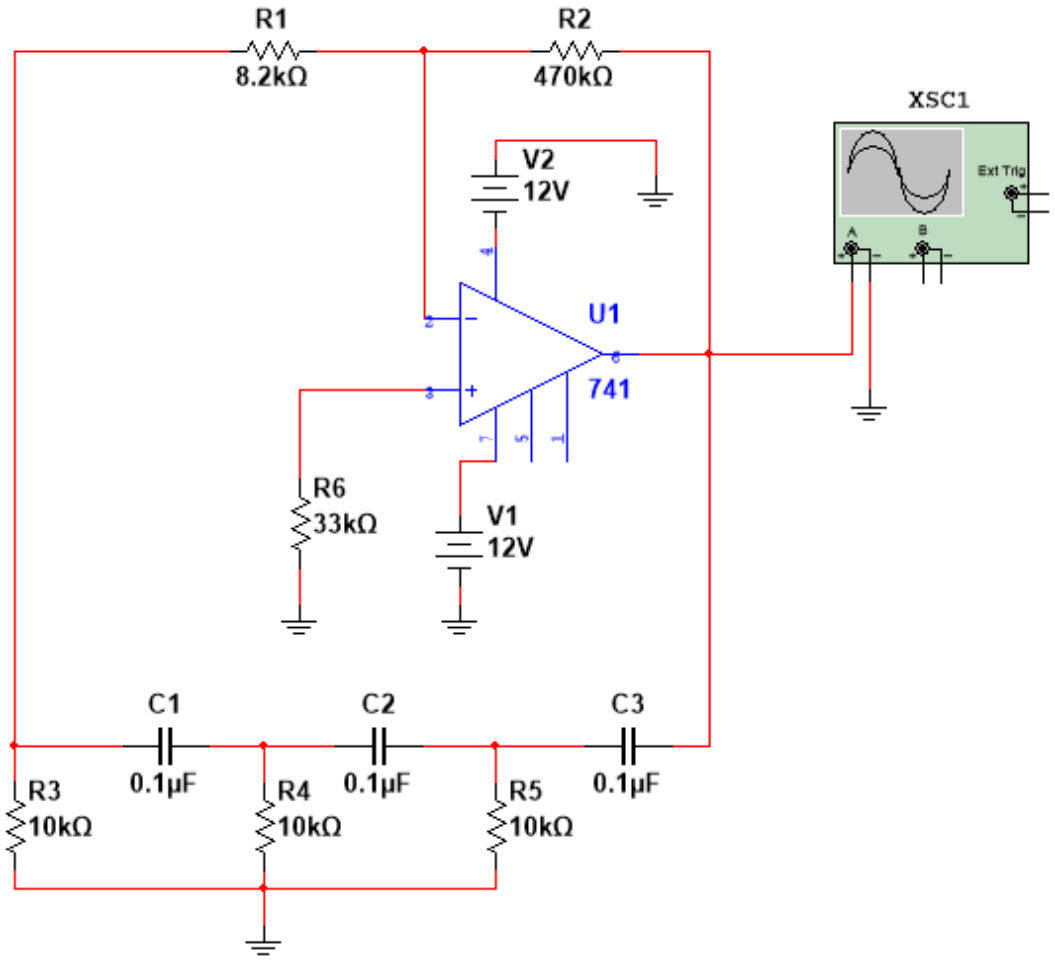
1. Connect the circuit as shown in the circuit diagram.
2. Observe the sinusoidal output on CRO.
3. Measure the time period of the sinusoidal wave and calculate its frequency.
4. Compare the measured frequency with $f = 0.065/\mathrm{RC}$.

RESULT & DISCUSSION:

PRECAUTIONS:

1. Do not use open ended wires for connecting to 220V power supply.
2. Before connecting the power supply plug in to socket, ensure power supply should be switched-off.
3. Ensure all connections should tight before switching-on the power supply.
4. Power supply should be switched-off after completion of experiment.

EXPERIMENTAL SETUP:



(Circuit diagram for RC Phase Shift Oscillator using IC 741 OP-AMP)

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EXPERIMENT NO - 8

DESIGN OF INVERTING AND NON-INVERTING AMPLIFIER USING IC 741 OP-AMP AND FINDING ITS FREQUENCY RESPONSE

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM (A): Design of Inverting amplifier using IC 741 OP-AMP and finding its frequency response.

APPARATUS REQUIRED:

1. Microlab-II
2. Power Supply
3. Function Generator
4. AC Millivoltmeter

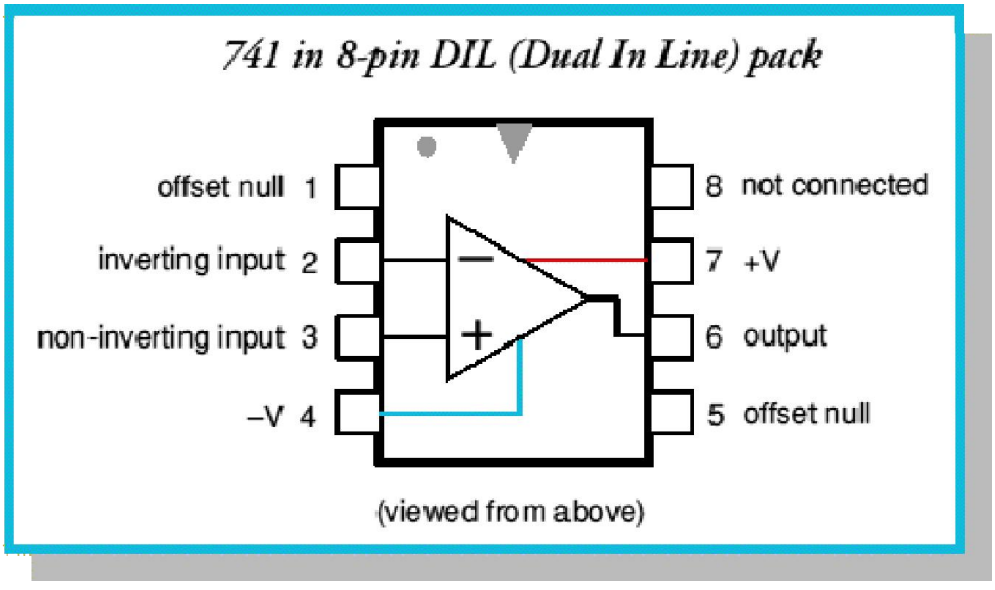
CIRCUIT COMPONENTS:

1. IC 741
2. Resistors 4.7KΩ, 47KΩ, 470KΩ

THEORY:

ABOUT OP-AMP IC 741

The 741 is the godfather of all operational amplifiers (amplifiers on a chip). Although most up-to-date designs beat it for speed, low noise, etc., it still works well as a general purpose device. One of its advantages is that it is *compensated* (its frequency response is tailored) to ensure that under most circumstances it won't produce unwanted spurious oscillations. This means it is easy to use, but the down-side of this is the poor speed/gain performance compared to more modern op-amps.



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popular that many other competing op-amps have adopted the same package/pinout. Hence for many applications the various op-amps are 'drop in' replacements or upgrades for one another. These days there is a large family of 741 type devices, made by various manufacturers. Sometimes one manufacturer will make different versions, which work better than others in some respect. Each has a slightly different part number, but it generally has "741" in it somewhere!

The values given below are 'typical' for an ordinary 741, better versions (more expensive) may give better results...

```
Typical values of Basic Parameters:
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      Input impedance: Around 2MegOhms
      Low Frequency voltage gain: approx. 200,000
      Input bias current: 80nA
      Slew rate: 0.5V per microsecond
      Maximum output current: 20mA
      Recommended output load: not less than 2kilOhms
```

Note that, due to the frequency compensation, the 741's voltage gain falls rapidly with increasing signal frequency. Typically down to 1000 at 1kHz, 100 at 10kHz, and unity at about 1MHz. To make this easy to remember we can say that the 741 has a *gain-bandwidth product* of around one million (i.e. 1 MHz as the units of frequency are Hz).

INVERTING OPERATIONAL AMPLIFIER CONFIGURATION:

In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V2 always equals V3". However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **"Virtual Earth/Ground"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, R1 and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as V3 = V2 = 0 (Virtual Earth)

The basic circuit of Inverting amplifier is shown below. In this mode of operation the positive input terminal of the amplifier is grounded and the input signal V_{in} is applied to the negative input terminal via resistor R1. The feedback applied through Rf = R2 from the input terminal, is negative. This helps to in maintaining gain stable. The inverting

operation performed by circuit is determined by Rf=R2 & R1. Note that the resistor R2 provides the negative feedback. Since the input signal is applied to the inverting input (–), the output will be inverted (i.e. 180° out of phase) as compared to the input. Hence the name inverting amplifier.

Referring to Fig., the current to the inverting input is zero. Therefore, current I_{in} flowing through R1 entirely flows through feedback resistor R2. In other words, $I_f = I_{in}$.

Thus, $I_{in} = \frac{V_{in}-0}{R1} = I_f = \frac{0-V_{out}}{R2}$

Since, $I_{in} = I_f \Longrightarrow \frac{V_{in}}{R1} = \frac{-V_{out}}{R2}$

Thus, the Closed-loop voltage gain $A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R2}{R1}$

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Keep R1=4.7KΩ, Rf = R2= 470KΩ
3. Keep Vin = 100mV fixed.
4. Vary the frequency from 10Hz onwards and note down the output reading at each time keeping Vin =100mV (fixed) and tabulate the readings in to observation table.
5. Plot Gain (dB) against frequency on semi-logarithmic graph sheet.
6. Repeat steps 2 to 5 for R1=47KΩ again.
7. Find 3dB point frequencies and Bandwidth.
8. Compare the Gain-Bandwidth product for 4.7 KΩ and 47 KΩ resistance.
9. Observe the input and output waveforms for a single frequency in mid-band range.

Note: Try to take the reading until gain will drop from its constant gain up to the value, which is approximately equal to the gain value for first reading.

OBSERVATIONS:

Input Voltage (fixed) V_{in} = 100 mV

Frequency (Hz)	Output Voltage V_{out} (Volt)	Voltage Gain (V_{out}/ V_{in})	Gain [20 $\log_{10}$ (V_{out}/V_{in})] (dB)
10			
20			

100			
200			

1K			
2K			
3K			

10K			
20K			

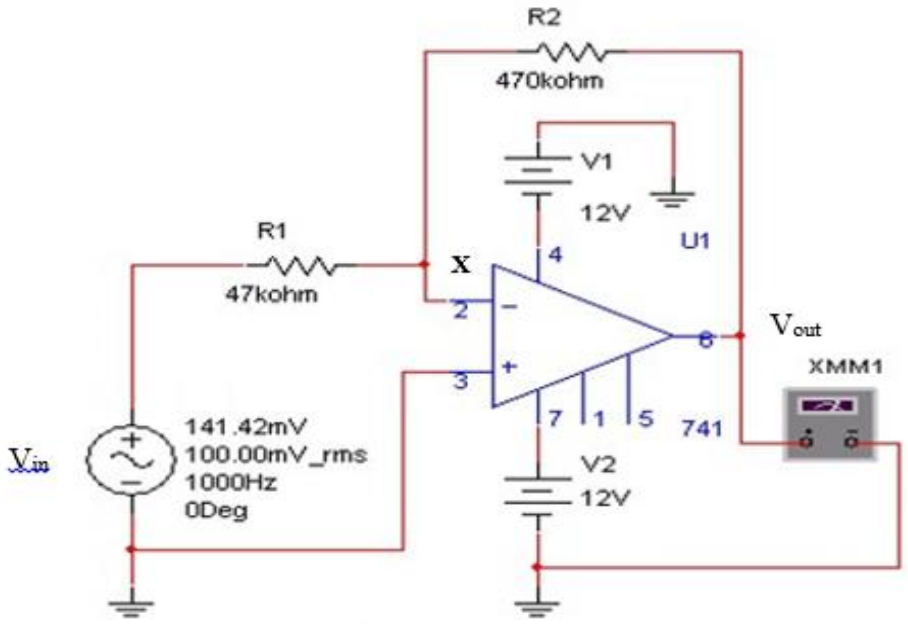
100K			
200K			

RESULT & DISCUSSION:

PRECAUTIONS:

1. Make the connections according to the pin-diagram and switch on the power supply.
2. The connections should be tight.
3. The V_{CC} and ground should be applied carefully at the specified pin only.
4. Readings should be taken carefully.

EXPERIMENTAL SETUP:



(Circuit diagram of Inverting amplifier using IC 741 OP-AMP)

AIM (B): Design of Non-Inverting amplifier using IC 741 OP-AMP and finding its Frequency response.

APPARATUS REQUIRED:

1. Microlab-II
2. Power Supply
3. Function Generator
4. AC Millivoltmeter

CIRCUIT COMPONENTS:

1. IC 741
2. Resistors 47KΩ, 470 KΩ

THEORY:

NON-INVERTING OPERATIONAL AMPLIFIER

It is called as non-inverting amplifier because input is applied at pin no.3 i.e. non-inverting input. So we get output-signal in phase with input signal. In this case the input-signal is applied directly to the non-inverting (+ve) input-terminal of the amplifier & the feedback resistor 'R2 = Rf' is connected between the output-terminal & negative input-terminal. The 'R1' is connected between the inverting terminal & ground. Note that V_{in} is not equal to zero in this case, meaning that non-inverting circuit has to virtual ground at one of its input-terminals. Thus the closed loop gain of a non-inverting amplifier is always greater than or equal to unity & it is determined by R1 & Rf.

Voltage gain

If we assume that we are not at saturation, the potential at point X is the same as V_{in}. Since the input impedance of OP-amp is very high, all of the current that flows through R2, also flows through R1. Thus, we have,

Voltage across R1=V_{in}-0 and Voltage across R2 = V_{out} -V_{in}

Now, current through R1=Current through R2

$$\therefore \quad \frac{V_{in}-0}{R1}=\frac{V_{out}-V_{in}}{R2}$$

$$\Longrightarrow \quad V_{in}.R2=V_{out}.R1-V_{in}.R1$$

Thus, the Closed-loop voltage-gain $A_{CL} = \frac{V_{out}}{V_{in}} = \frac{R2 + R1}{R1} = 1 + \frac{R2}{R1}$

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a R2 – R1 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, R_{in} approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, Rout.

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Keep R_1= 47 kΩ, R_f = R_2 = 470 kΩ,
3. Vary the frequency from 10Hz onwards and note down the output reading each time, keeping Vin=100 mV (fixed) and tabulate the reading in to observation table.
4. Plot Gain (dB) against frequency on semi-logarithmic graph sheet.
5. Find 3dB point frequencies and Bandwidth.
6. Observe the input and output waveforms for a single frequency in mid-band range.

Note: Try to take the reading until gain will drop from its constant gain up to the value, which is approximately equal to the gain value for first reading.

OBSERVATIONS:

Input Voltage (fixed) = 100 mV.

Frequency (Hz)	Output Voltage V_{out} (Volt)	Voltage Gain (V_{out}/ V_{in})	Gain [20 $\log_{10}$ (V_{out}/V_{in})] (dB)
10			
20			

100			
200			

1K			
2K			
3K			

10K			
20K			

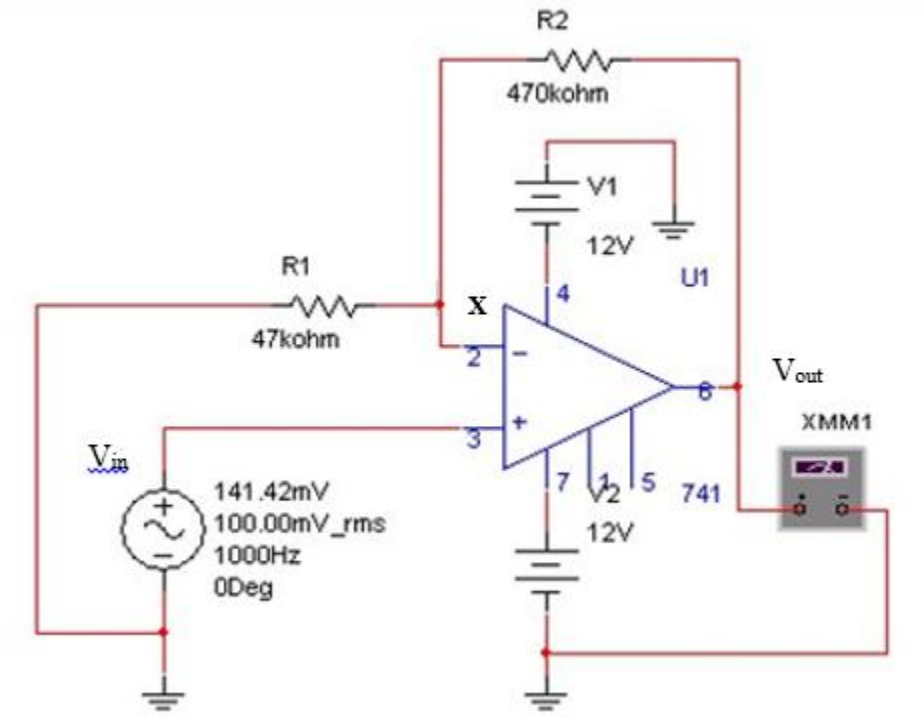
100K			
200K			

RESULT & DISCUSSION:

PRECAUTIONS:

1. Make the connections according to the pin-diagram and switch on the power supply.
2. The connections should be tight.
3. The V_{CC} and ground should be applied carefully at the specified pin only.
4. Readings should be taken carefully.

EXPERIMENTAL SETUP:



(Circuit diagram of Non-Inverting amplifier using IC 741 OP-AMP)

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EXPERIMENT NO - 9

REALIZATION OF BASIC LOGIC GATES (AND, OR, NOT) USING NAND GATE (IC 7400)

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Realization of Basic logic gates (AND, OR, NOT) using NAND Gate (IC 7400).

APPARATUS REQUIRED:

1. Bread Board/ Trainer Kit
2. D.C. Power Supply

CIRCUIT COMPONENTS:

1. IC7400
2. Connecting Wires

THEORY:

The NAND gate is said to be a universal gate because any all other gates as well as any digital system can be implemented with it. Combinational circuits and sequential circuits as well can be constructed with this gate because the flip-flop circuit can be constructed from two NAND gates connected back to back.

The NAND (Not – AND) gate has an output that is normally at logic level "1" and only goes "LOW" to logic level "0" when **ALL** of its inputs are at logic level "1". The **Logic NAND Gate** is the reverse or "*Complementary*" form of the AND gate. The logic or Boolean expression given for a logic NAND gate is that for *Logical Addition*, which is the opposite to the AND gate, and which it performs on the *complements* of the inputs. The Boolean expression for a logic NAND gate is denoted by a single dot or full stop symbol, (.) with a line or *Overline*, (¯) over the expression to signify the NOT or logical negation of the NAND gate giving us the Boolean expression of: $\overline{A.B} = Q$.

Then we can define the operation of a 2-input digital logic NAND gate as being:

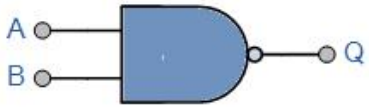
"If either A or B are NOT true, then Q is true"

Logic NAND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape is that of a standard AND gate with a circle, sometimes called an "inversion bubble" at its output to represent the NOT gate symbol with the logical operation of the NAND gate given as.

The implementation of the AND, OR, and NOT operations with NAND gates is shown in Fig. The NOT operation is obtained from a one-input NAND gate. The AND operation requires two NAND gates. The first produces the inverted AND and the second acts as an

inverter to produce the normal output. The OR operation is achieved through a NAND gate with additional inverters in each input.

2-input Logic NAND Gate

Symbol	Truth Table		
 2-input NAND Gate	B	A	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression $Q = \overline{A.B}$	Read as A **AND** B gives **NOT** Q		

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON power supply, make sure that the connection are correct.
3. Apply the input logic state code mentioned in Observation Table in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the output states.
5. Verify the result of truth ness.
6. Repeat steps from 3 to 5 for all possible combination.

OBSERVATIONS:

(i)Verifying: Truth Table of AND GATE

INPUT		OUTPUT
A	B	Y
0	0	
0	1	
1	0	
1	1	

(ii)Verifying: Truth Table of OR GATE

INPUT		OUTPUT
A	B	Y
0	0	
0	1	
1	0	
1	1	

(iii)Verifying: Truth Table of NOT GATE

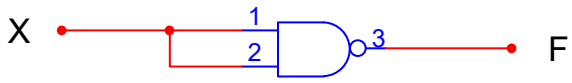
INPUT X	OUTPUT Y
0	
1	

RESULT & DISCUSSION:

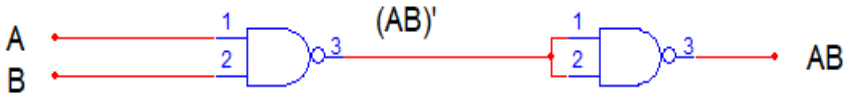
PRECAUTIONS:

1. Make the connections according to the pin-diagram and switch on the power supply.
2. The connections should be tight.
3. The V_{CC} and ground should be applied carefully at the specified pin only.
4. Readings should be taken carefully.

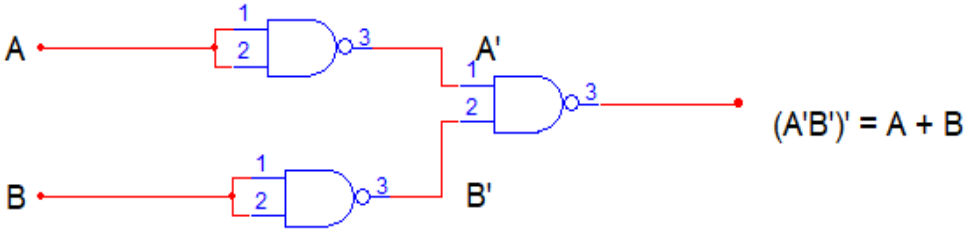
EXPERIMENTAL SETUP:



NOT GATE



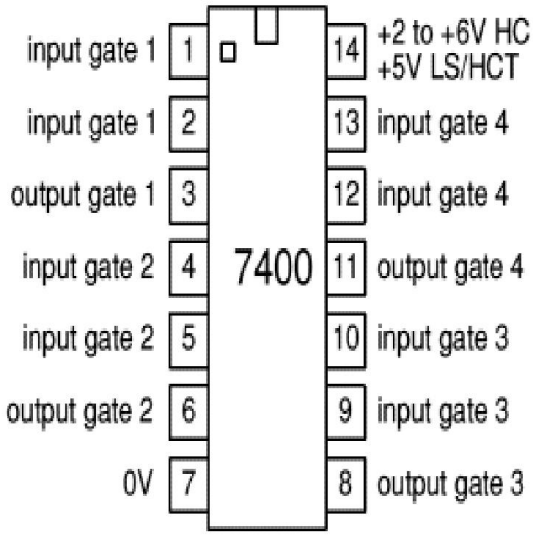
AND GATE



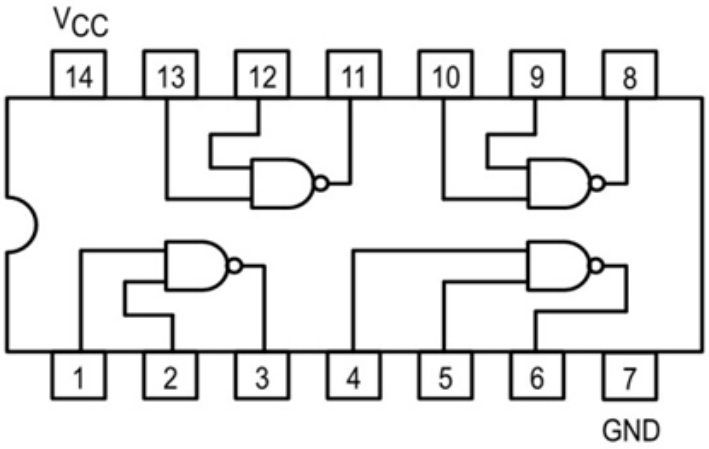
OR GATE

PIN DIAGRAM OF IC 7400

4 2-INPUTS NAND GATE



INTERNAL GATE CONNECTION OF IC 7400



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EXPERIMENT NO - 10

IMPLEMENTATION OF THE BOOLEAN EXPRESSION F = (A.B.C.D + D.E) USING AND-GATES (IC 7408) AND OR-GATE (IC 7432)

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Implementation of the Boolean Expression F = (A.B.C.D + D.E) using AND Gates (IC 7408) and OR Gate (IC 7432).

APPARATUS REQUIRED:

1. Bread Board/ Trainer Kit
2. D.C. Power Supply

CIRCUIT COMPONENTS:

1. IC 7408
2. IC 7432
3. Connecting Wires

THEORY:

AND Gate

The output state of a "Logic AND Gate" only returns "LOW" again when **ANY** of its inputs are at a logic level "0". In other words for a logic AND gate, any LOW input will give a LOW output.

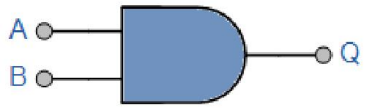
The logic or Boolean expression given for a digital logic AND gate is that for *Logical Multiplication* which is denoted by a single dot or full stop symbol, (.) giving us the Boolean expression of: A.B = Q.

Then we can define the operation of a 2-input logic AND gate as being:

"If both A and B are true, then Q is true"

Logic AND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the AND gate.

The 2-input Logic AND Gate

Symbol	Truth Table		
 2-input AND Gate	B	A	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression **Q = A.B**	Read as A **AND** B gives Q		

OR Gate

The output, Q of a "Logic OR Gate" only returns "LOW" again when **ALL** of its inputs are at a logic level "0". In other words for a logic OR gate, any "HIGH" input will give a "HIGH", logic level "1" output.

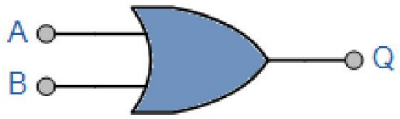
The logic or Boolean expression given for a digital logic OR gate is that for *Logical Addition* which is denoted by a plus sign, (+) giving us the Boolean expression of: A+B = Q.

Thus a logic OR gate can be correctly described as an "Inclusive OR gate" because the output is true when both of its inputs are true (HIGH). Then we can define the operation of a 2-input logic OR gate as being:

"If either A or B is true, then Q is true"

Logic OR Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the OR gate.

The 2-input Logic OR Gate

Symbol	Truth Table		
 2-input OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression **Q = A+B**	Read as A **OR** B gives Q		

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON Power Supply, make sure that the connections are correct.
3. Apply the input logic as per Truth Table in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the output states.
5. Verify the result of truth ness.
6. Repeat steps from 3 to 5 for all possible combinations.

OBSERVATIONS:

FUNCTION TABLE

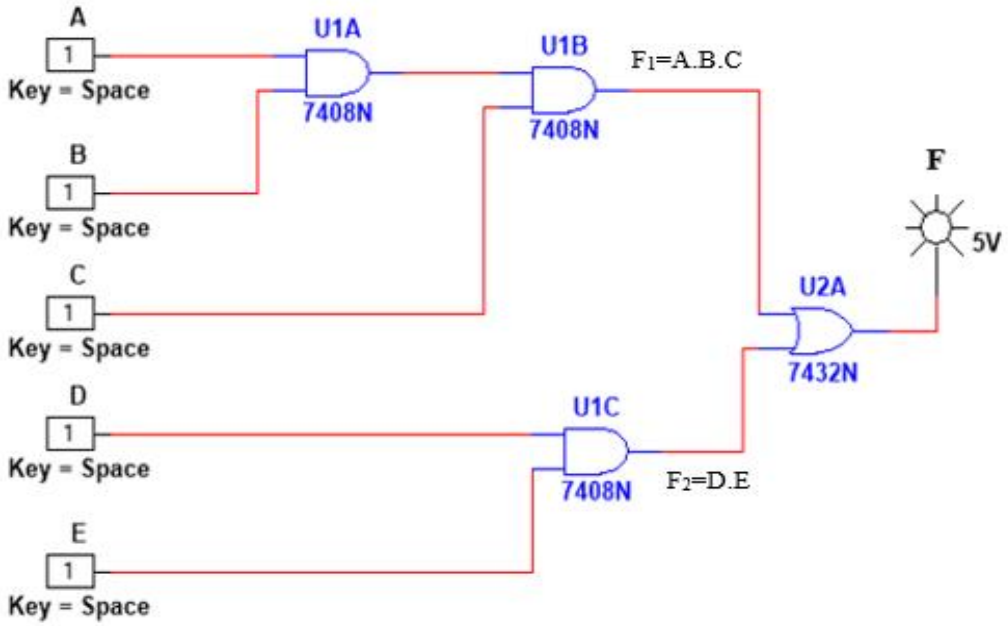
INPUTS					INTERMEDIATE FUNCTIONS		FINAL OUTPUT
A	B	C	D	E	F_1 = A.B.C	F_2=D.E	F=A.B.C + D.E

RESULT & DISCUSSION:

PRECAUTIONS:

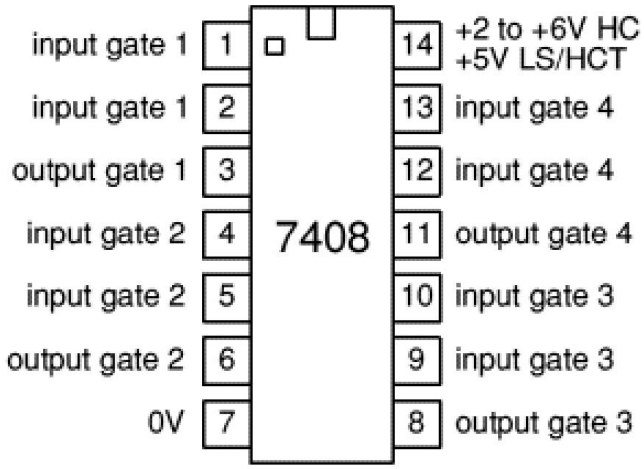
1. Make the connections according to the pin-diagram and switch on the power supply.
2. The connections should be tight.
3. The V_{CC} and ground should be applied carefully at the specified pin only.
4. Readings should be taken carefully.

EXPERIMENTAL SETUP:

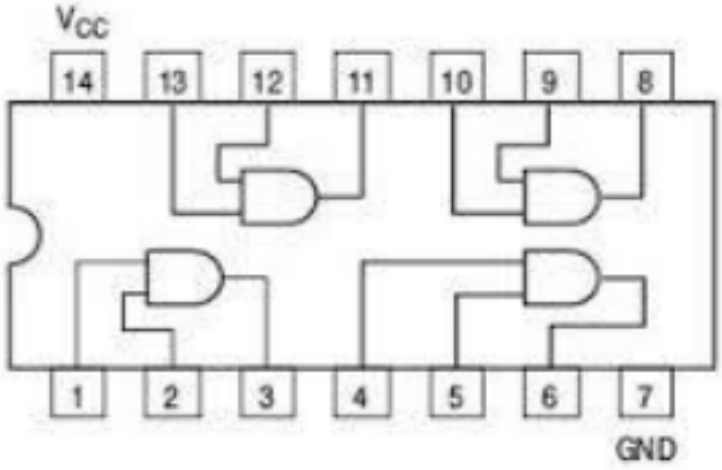


PIN DIAGRAM OF IC 7408

QUAD 2 INPUTS AND GATE

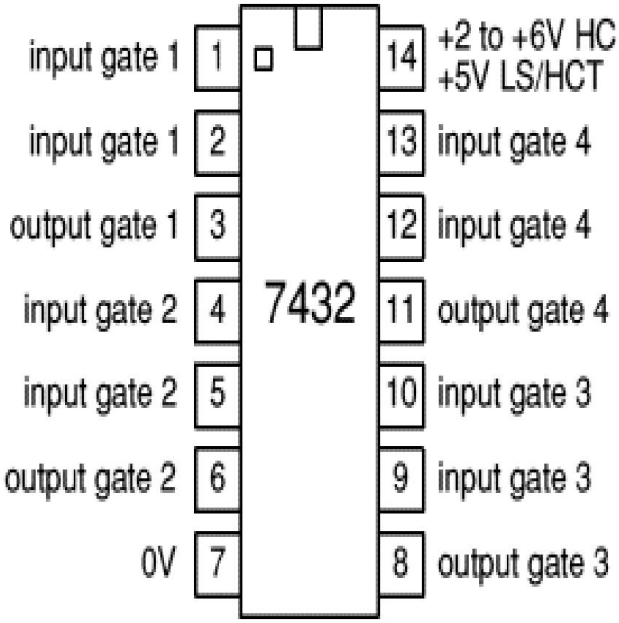


NTERNAL GATE CONNECTION OF IC 7408

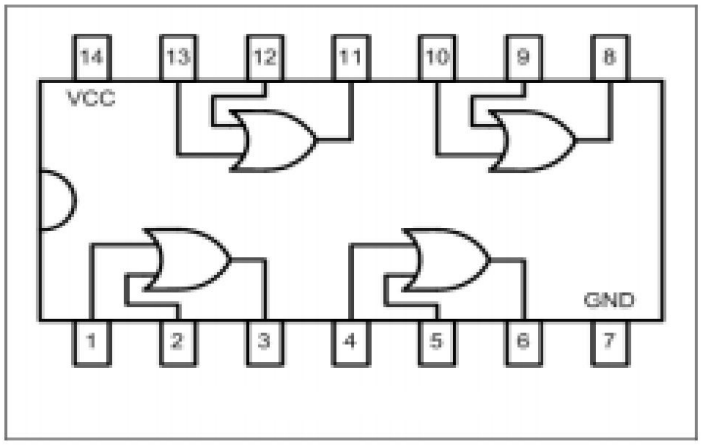


PIN DIAGRAM OF IC 7432

QUAD 2 INPUTS OR GATE



INTERNAL GATE CONNECTION OF IC 7432



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EXPERIMENT NO - 11

GENERATION OF AMPLITUDE MODULATED WAVE AND CALCULATION OF PERCENTAGE OF MODULATION USING STANDARD SETUP

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Generation of Amplitude modulated wave and calculation of percentage of modulation using standard setup.

SOFTWARE USED: Embed SE 2017.2 Software

THEORY:

Amplitude Modulation is defined as a process in which the amplitude of the carrier wave C(t) is varied linearly with the instantaneous amplitude of the message signal m(t).The standard form of an amplitude modulated (AM) wave is defined by;

$$S(t) = A_C[1 + K_a m(t)] \cos 2\pi f_C t$$

Where Ka is a constant called the amplitude sensitivity of the modulator.

The demodulation circuit is used to recover the message signal from the incoming AM wave at the receiver. An envelope detector is a simple and yet highly effective device that is well suited for the demodulation of AM wave, for which the percentage modulation is less than 100%. Ideally, an envelope detector produces an output signal that follows the envelop of the input signal wave form exactly; hence, the name. Some version of this circuit is used in almost all commercial AM radio receivers.

The Modulation Index is defined as,

$$m = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}$$

Where Emax and Emin are the maximum and minimum amplitudes of the modulated wave.

PROCEDURE:

1. Connect the circuit as per the circuit diagram shown in Fig.
2. Apply sinusoidal signal of 1 Hz frequency and amplitude 2 Vp-p as modulating signal and carrier signal of frequency 10 Hz and amplitude 6 Vp-p.
3. Now slowly increase the amplitude of the modulating signal to 1.5 V and 2 V, keeping carrier signal of frequency 10 Hz and amplitude 6 Vp-p constant.
4. Note down values of Emax and Emin in all the three cases.
5. Calculate modulation index using formula.
6. Apply the multi-tone signal (taking combination of all three modulating signals above) as modulating signal and carrier signal of frequency 10 Hz and amplitude 10 Vp-p.
7. Observe the time-domain of the AM-modulated and demodulated signal for the multi-tone modulating signal and plot them.

8. Observe the frequency-domain of the AM-modulated and demodulated signal for the multi-tone modulating signal and plot them.

OBSERVATIONS:

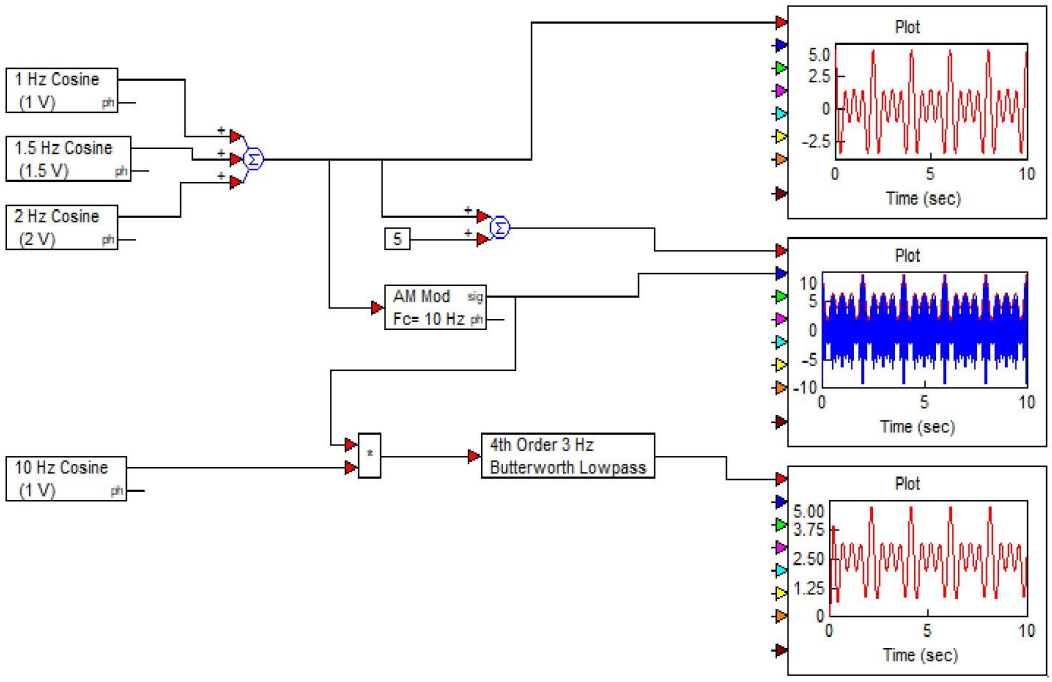
SL. NO.	A_m (V)	E_{max} (V)	E_{min} (V)	%age of modulation (m)
1.	1 V			
2.	1.5 V			
3.	2 V			

RESULT & DISCUSSION:

PRECAUTIONS:

1. Make the connection of different modules as per the circuit diagram given.
2. Observations should be done carefully.

EXPERIMENTAL SETUP:



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EXPERIMENT NO - 12

GENERATION OF FM-WAVE AND ITS DETECTION USING STANDARD SETUP

BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

AIM: Generation of FM-wave and its detection using standard setup.

SOFTWARE USED: Embed SE 2017.2 Software

THEORY:

The process, in which the frequency of the carrier is varied in accordance with the instantaneous amplitude of the modulating signal, is called "Frequency Modulation". The FM signal is expressed as;

$$S(t) = A_C \cos[2\pi f_C t + \beta \sin(2\pi f_m t)]$$

Where A_C is amplitude of the carrier signal, f_C is the carrier frequency β is the modulation index of the FM wave.

Where, modulating signal, $m(t) = A_m \cos(2\pi f_m t)$
and carrier signal, $C(t) = A_C \cos(2\pi f_C t)$

The instantaneous frequency of the resulting FM wave is,

$$\begin{aligned} f_i(t) &= f_C + K_f\, m(t) \\ &= f_C + K_f A_m \cos(2\pi f_m t) \\ &= f_C + \Delta f \cos(2\pi f_m t) \end{aligned}$$

Where, $\Delta f = K_f A_{m=}$ frequency deviation. It is the maximum departure of the instantaneous frequency of the FM wave from the carrier frequencyf_C. A fundamental characteristic of FM wave is that the Δf is propotional to the amplitude of the modulating signal.

The constant term f_C represents the frequency of the unmodulated carrier; the constant K_f represents the frequency-sensitivity factor of the modulator, expressed in hertz per volt on the assumption that is a voltage waveform. Integrating Eq.- $f_i(t)$ with respect to time and multiplying the result by 2π we get

$$\begin{aligned} \theta_i(t) &= 2\pi \int_0^t f_i(t).\, dt \\ &= 2\pi f_C t + 2\pi K_f \int_0^t m(t).\, dt \\ &= 2\pi f_C t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \\ &= 2\pi f_C t + \beta \sin(2\pi f_m t) \end{aligned}$$

The parameter $\beta = modulation\ index = \frac{\Delta f}{f_m}$, represents the phase deviation of the FM wave that is the maximum departure of the angle $\theta_i(t)$ from the angle $2\pi f_C t$ of the unmodulated carrier. Depending on the $\beta - value$, there are two cases;

1. Narrow-Band FM (for β very small value)
2. Wide-Band FM (for β very large value)

PROCEDURE:

1. Connect the circuit as per the circuit diagram shown in Fig.
2. Apply sinusoidal signal of 1 Hz frequency and amplitude 2 Vp-p as modulating signal, and carrier signal of frequency 5 Hz and amplitude 2 Vp-p.
3. Observe the time-domain of FM-modulated and demodulated signals and plot them.
4. Observe the frequency-domain of FM-modulated and demodulated signals and plot them.

RESULT & DISCUSSION:

PRECAUTIONS:

1. Make the connection of different modules as per the circuit diagram given.
2. Observations should be done carefully.

EXPERIMENTAL SETUP: